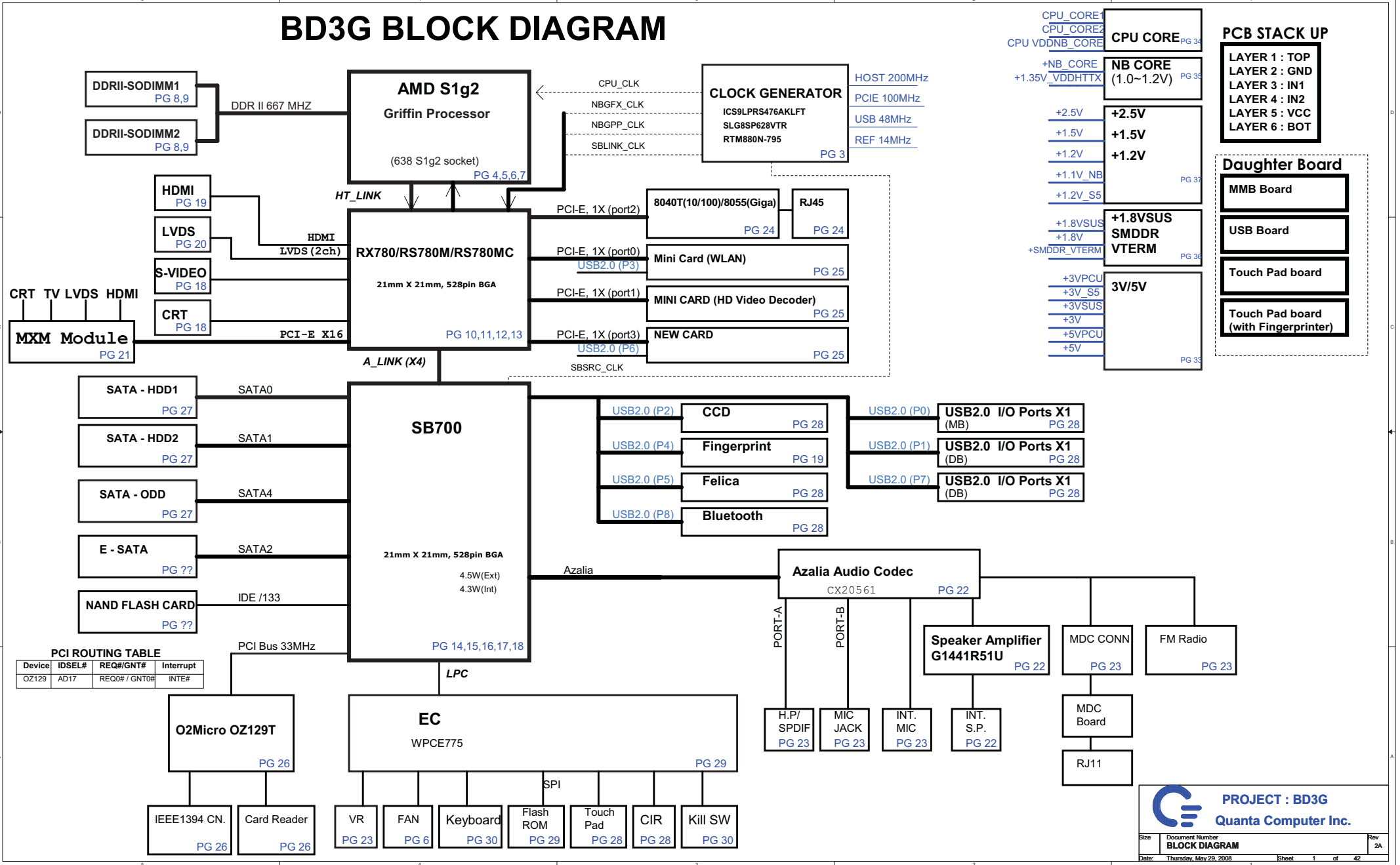


BD3G BLOCK DIAGRAM



CPU_CORE1	CPU CORE	PG 34
CPU_CORE2	CPU CORE	PG 34
CPU_VDDNB_CORE	CPU CORE	PG 34
+NB_CORE	NB CORE	(1.0~1.2V) PG 35
+1.35V_VDDHTTX		
+2.5V	+2.5V	
+1.5V	+1.5V	
+1.2V	+1.2V	
+1.1V_NB		PG 37
+1.2V_S5		
+1.8VSUS	+1.8VSUS	
+1.8V	SMDDR	
+SMDDR_VTERM	VTERM	PG 36
+3VPCU	3V/5V	
+3V_S5		
+3VSUS		
+3V		
+5VPCU		
+5V		PG 35

PCB STACK UP

LAYER 1 : TOP
 LAYER 2 : GND
 LAYER 3 : IN1
 LAYER 4 : IN2
 LAYER 5 : VCC
 LAYER 6 : BOT

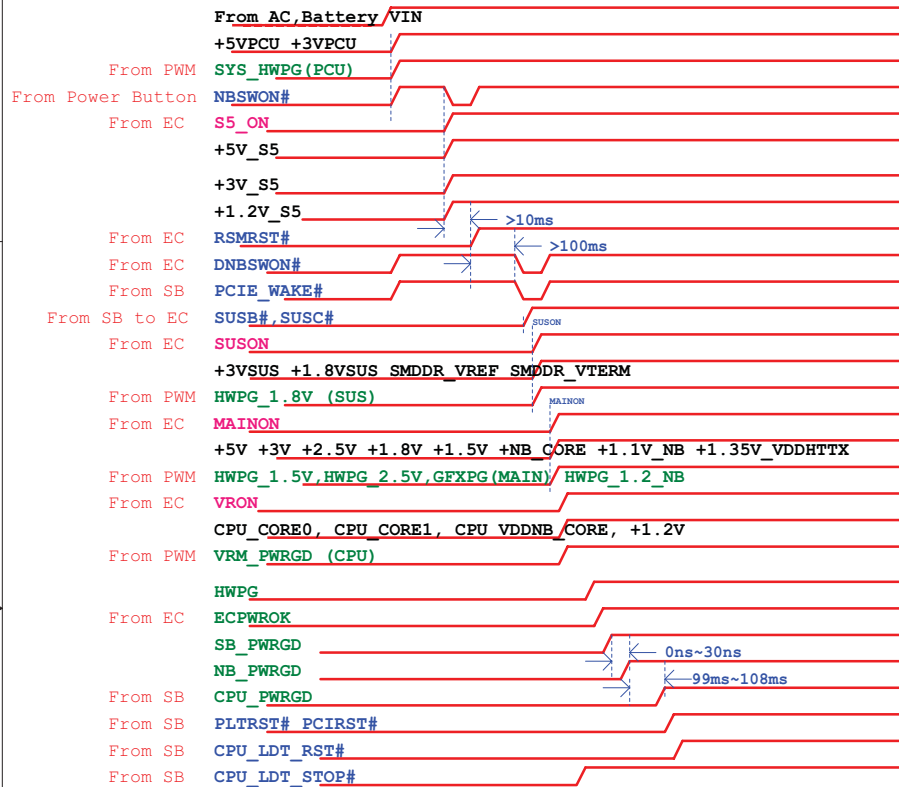
Daughter Board

MMB Board
 USB Board
 Touch Pad board
 Touch Pad board (with Fingerprinter)

PCI ROUTING TABLE

Device	IDSEL#	REQ#/GNT#	Interrupt
OZ129	AD17	REQ0# / GNT0#	INTE#

BD3G Power On Sequence



*Note: EC will sampling SUSB# & SUSC# every 5ms.

AMD SB700 SMBUS Table

	CLK GEN	RAM	Mini Card (HD-Decoder)	Mini-card (WL)	New Card	HDMI
SB700 SDATA0/SCLK0 (+3V)	V	V	V	V	V	
SB700 SDATA1/SCLK1 (+3V_S5)						V
SB700 SDATA2/SCLK2 (+3V_S5)						
Power	+3V	+3V	+3V	+3V (Atheros)	+3V	+3V_S5
Reserve MOS ckt	V	V	V	V	V	V

BOM naming rule

Items	Function	BTO	Name	Description
1	CIR	v	CIR@	
2	HDMI port	v	HDM@	
3	HDMI transmitter	v	SI@	Silicon image SiI 1392/1932
4	HDMI-CEC	v	CEC@	Renesas R8C/1B
5	Discrete VGA		EV@	External VGA stuff
6	UMA		IV@	Internal VGA stuff
7	New Card		NEW@	
8	RJ11	v	MD@	Modem
9	RJ45-10/100		40@	Marvell 8040T(10/100)
10	RJ45-1000		55@	Marvell 8055(Giga)
11	Option for RJ45-10/100 and RJ45-1000		40@55@	Option for 8040/8055
12	TV	v	TV@	
13	Cardbus		CB@	
14	FM transmitter	v	FM@	
15	Mainstream ID LED		MID@	
16	Low cost ID LED		LID@	
17	CCD	v	CCD@	
18	INT MIC	v	I_MIC@	
19	AMD Hyper Flash		HF@	Only for AMD platform
20	North bridge(690MC/RS780MC)		MC@	Only for AMD platform
21	North bridge(RX780)		RX@	Only for AMD platform
22	PowerXpress		PX@	Only for AMD platform
23	PowerXpress with UMA SKU		PX@IV@	Only for AMD platform
24	PowerXpress with Discrete VGA SKU		PX@EV@	Only for AMD platform
25	Power player/Power Shift		PP@	Only for AMD platform

EC SMBUS Table

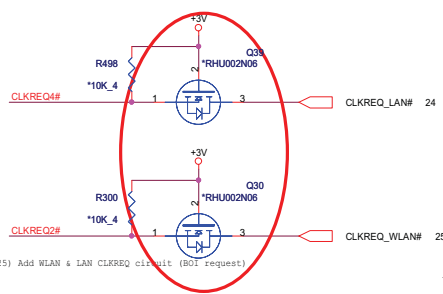
	Battery	CPU thermal Sensor	EC EEPROM	VGA thermal Sensor	Touch Sensor	HDMI CEC
EC775 SDATA1/SCLK1 (+3VPCU)	v					
EC775 SDATA2/SCLK2 (+3VPCU)		v	v			
EC775 SDATA3/SCLK3 (+3VPCU)				v	v	v
EC775 SDATA4/SCLK4 (+3VPCU)						
Power	+3VPCU	+3V	+3VPCU	+3V	+3VPCU	+5VPCU
Reserve MOS ckt	X	v	X	v	X	v



ICS9LPRS480 P/N : ALPRS480000
 SLG8SP628 P/N : AL8SP628000
 RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

10/25 modify it



B: (10/25) Add WLAN & LAN CLKREQ circuit (B01 request)

12/8 change from 20p to 33p

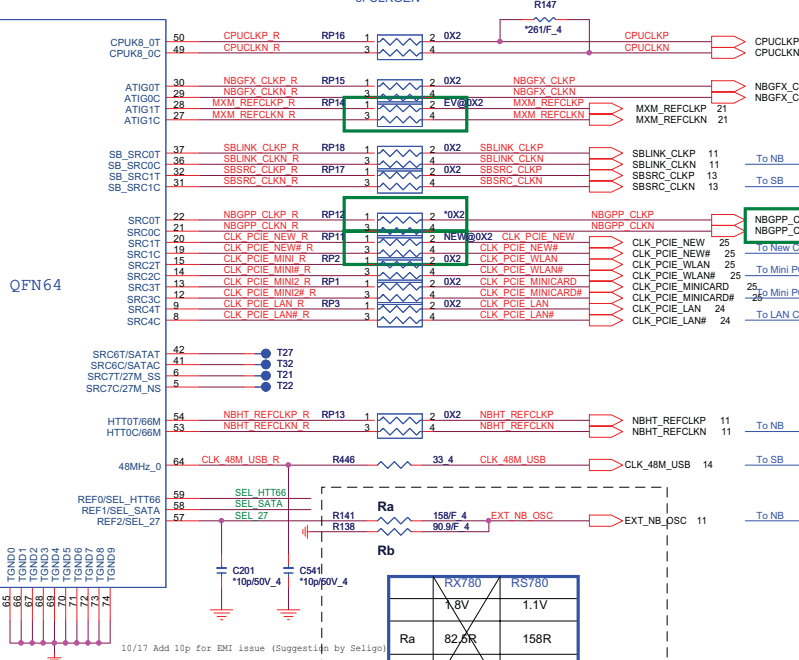


CLOCKS name	RX780	RS780	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	RP1001 STUFF	RP1001 STUFF	to NB for VGA reference clock
MXM_REFCLKP MXM_REFCLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NB_GPP_CLKP NB_GPP_CLKN	RP1005 STUFF	RP1005 NC	to NB for RX780 for PCIeX2 interface reference clock only RS780 is internal share with AC-LINK clock, RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP1003 STUFF	RP1003 STUFF	to NB for AC-LINK reference clock

U2

QFN64

SLG8SP628



Place within 0.5" of CLKGEN

To CPU

RS780/RX780 for VGA

To NB

11/4 check RX781, RX781 not use

RX780 only

To NB

NB CLOCK INPUT TABLE

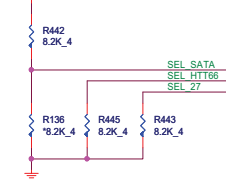
NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLKN	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

	RX780	RS780
Ra	158R	1.1V
Rb	130R	90.9R

RES CHIP 130 1/16W +/-1%(0402)LF -->CS11302FB15
 RES CHIP 158 1/16W +/-1%(0402) -->CS11582FB00
 RES CHIP 90 9 1/16W +/-1%(0402) -->CS0902FB15
 RES CHIP 82.5 1/16W +/-1%(0402) -->CS0825FB11

10/17 Add 10p for EMI issue (Suggestion by Seigo)

+3V_CLK_VDD

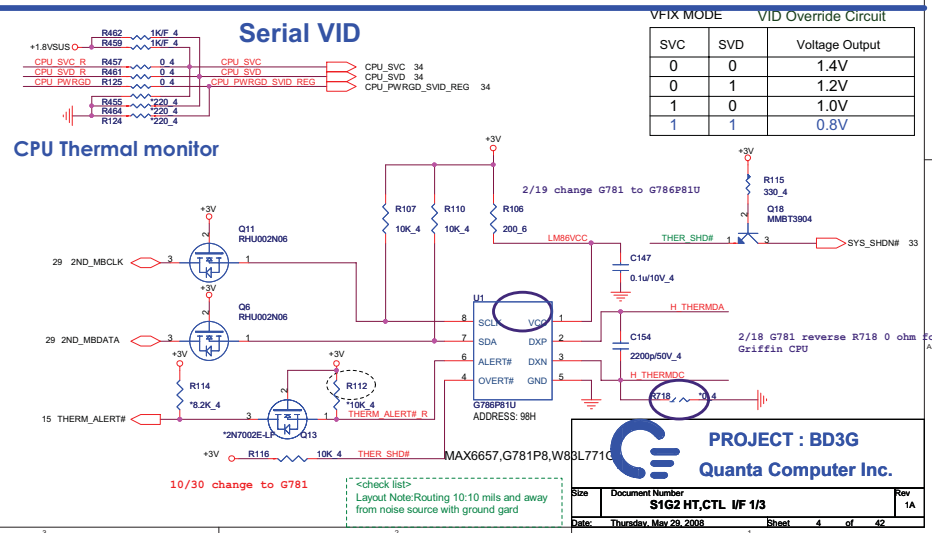
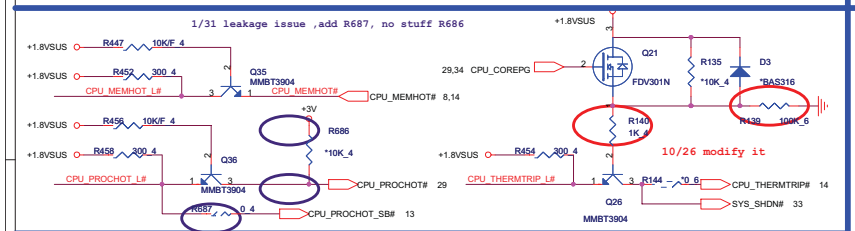
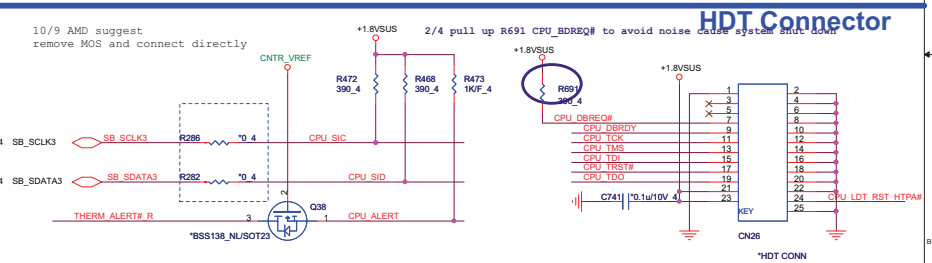
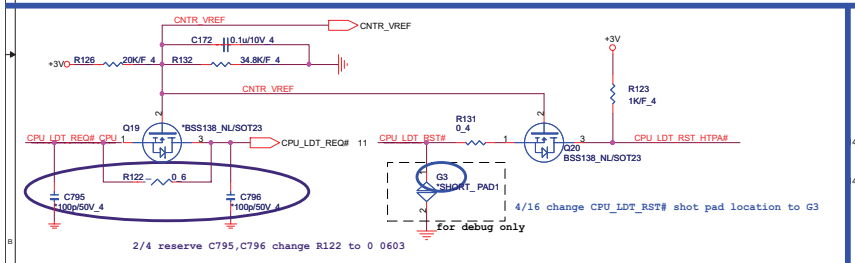
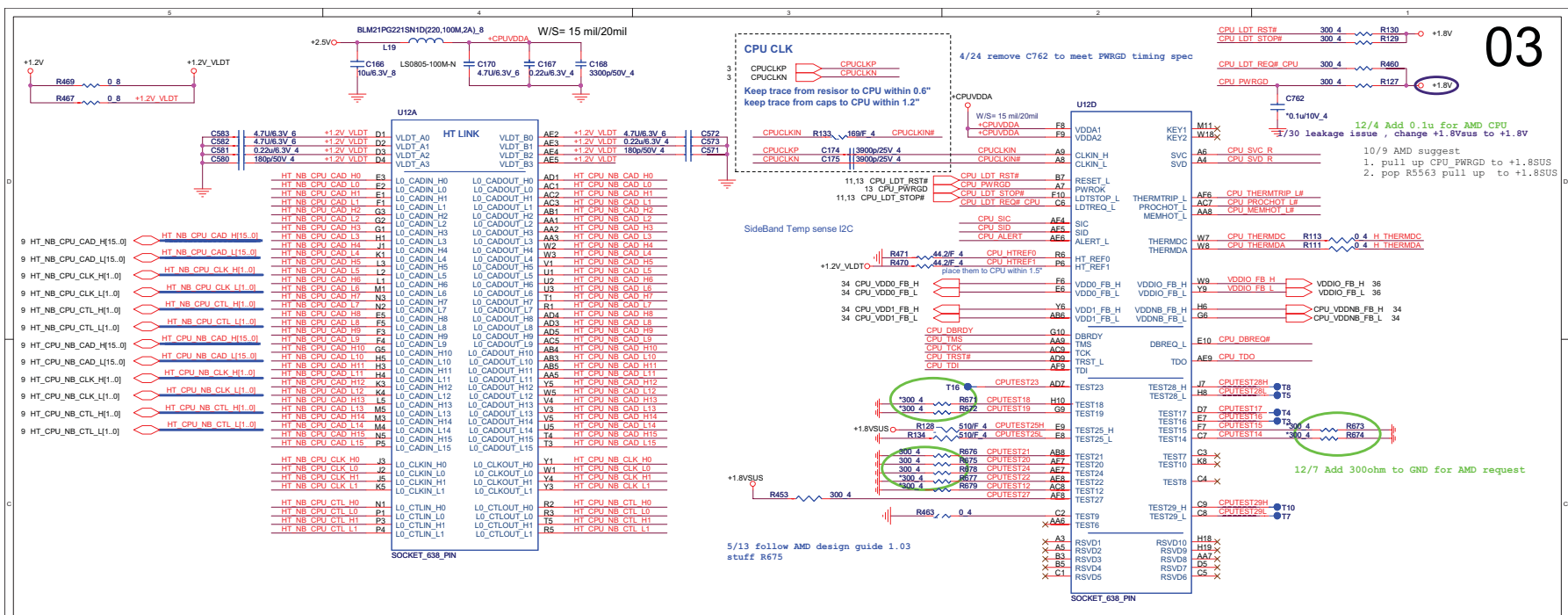


SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
SEL_SATA	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
SEL_SATA	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
SEL_27	0*	100 MHz SRC clock

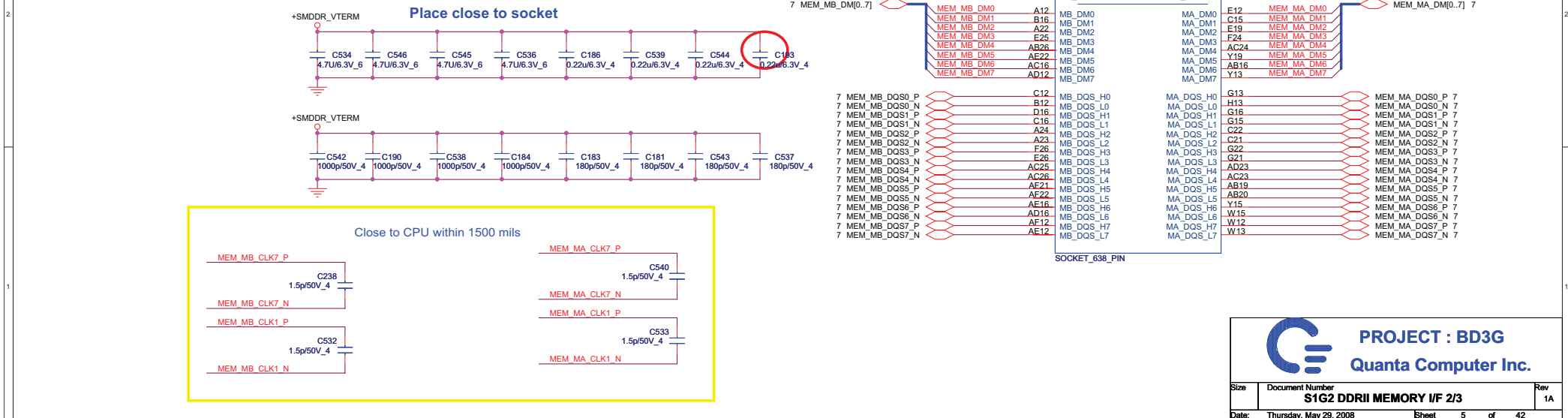
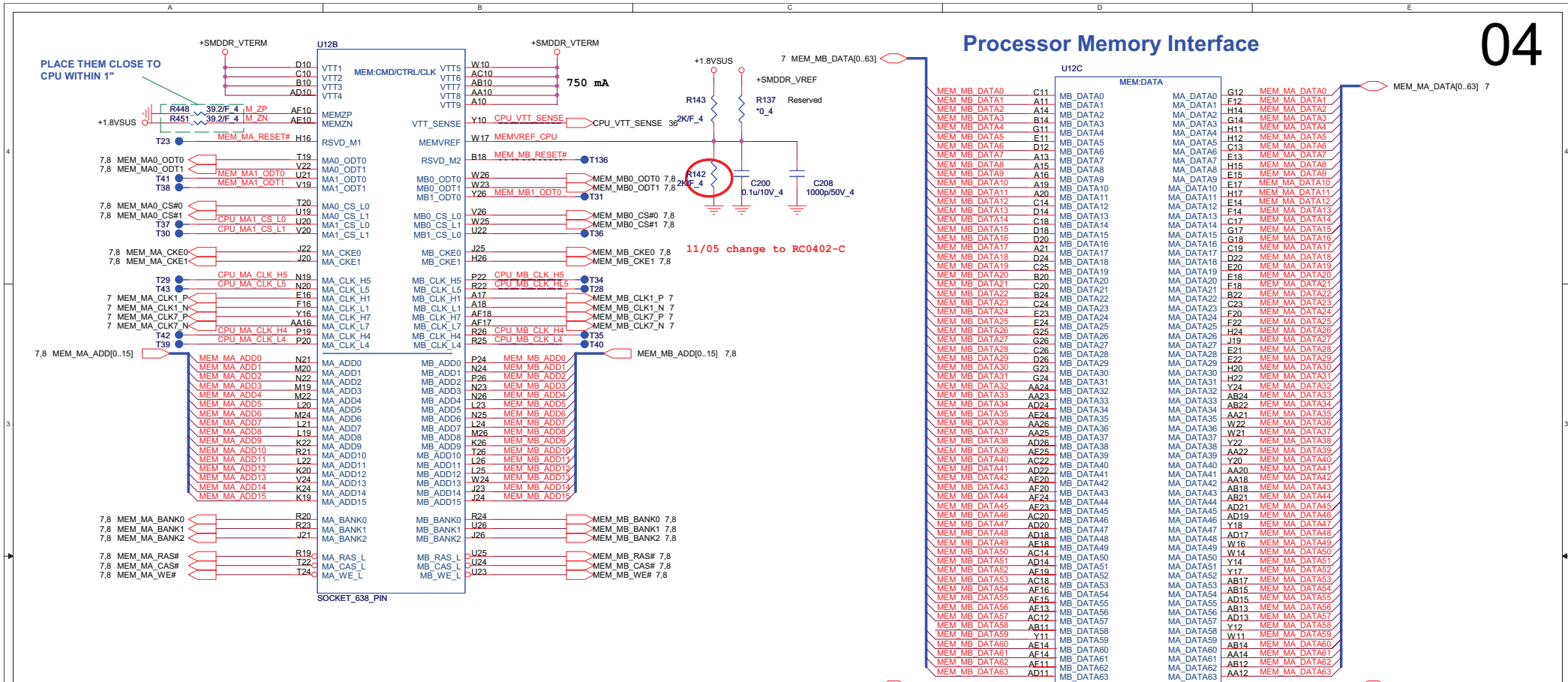
* default

PROJECT : BD3G
Quanta Computer Inc.

Size: 200 Document Number: **CLOCK GENERATOR_SLG8SP628** Rev: 1A
 Date: Thursday, May 29, 2008 Sheet: 3 of 42

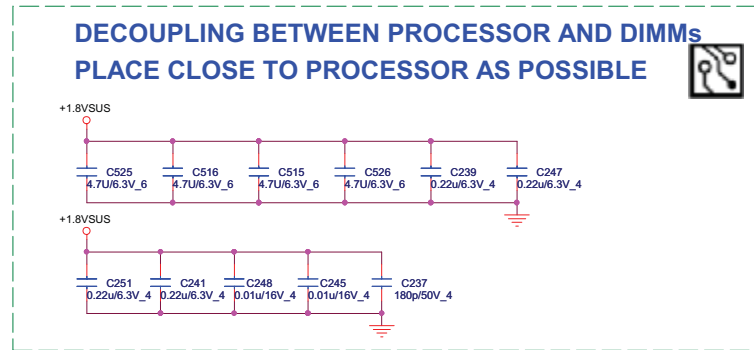
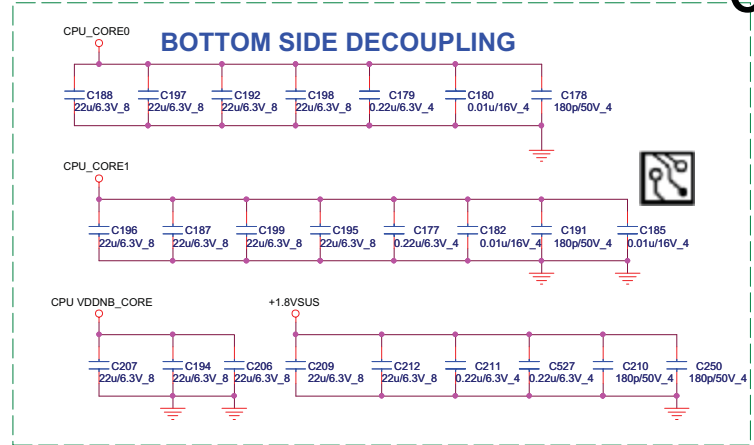
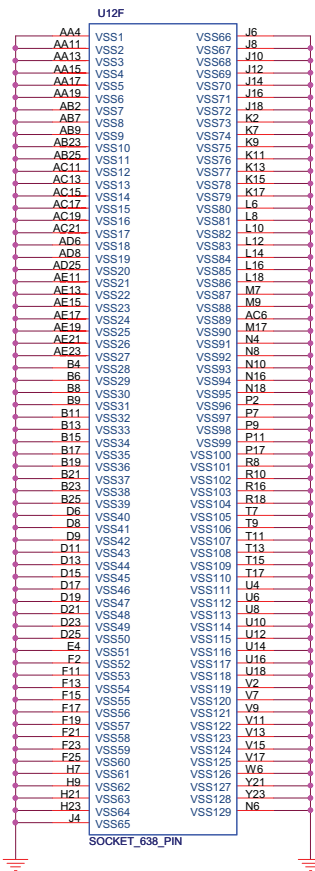
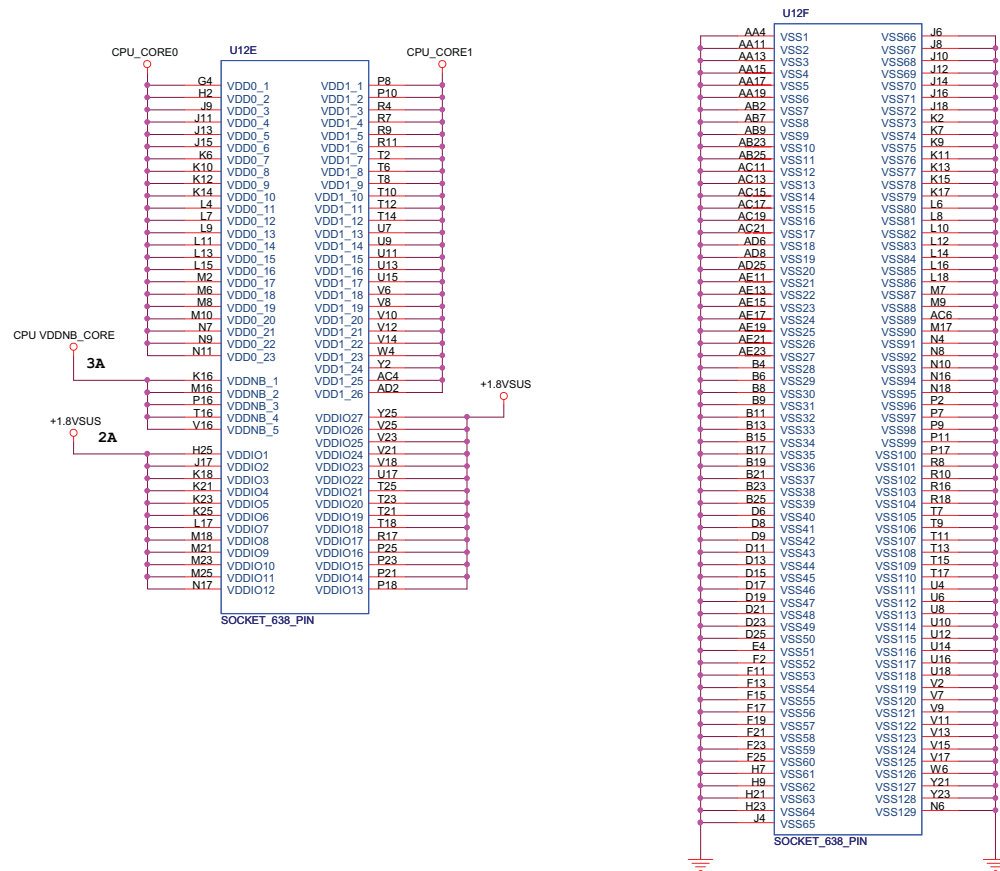


Processor Memory Interface

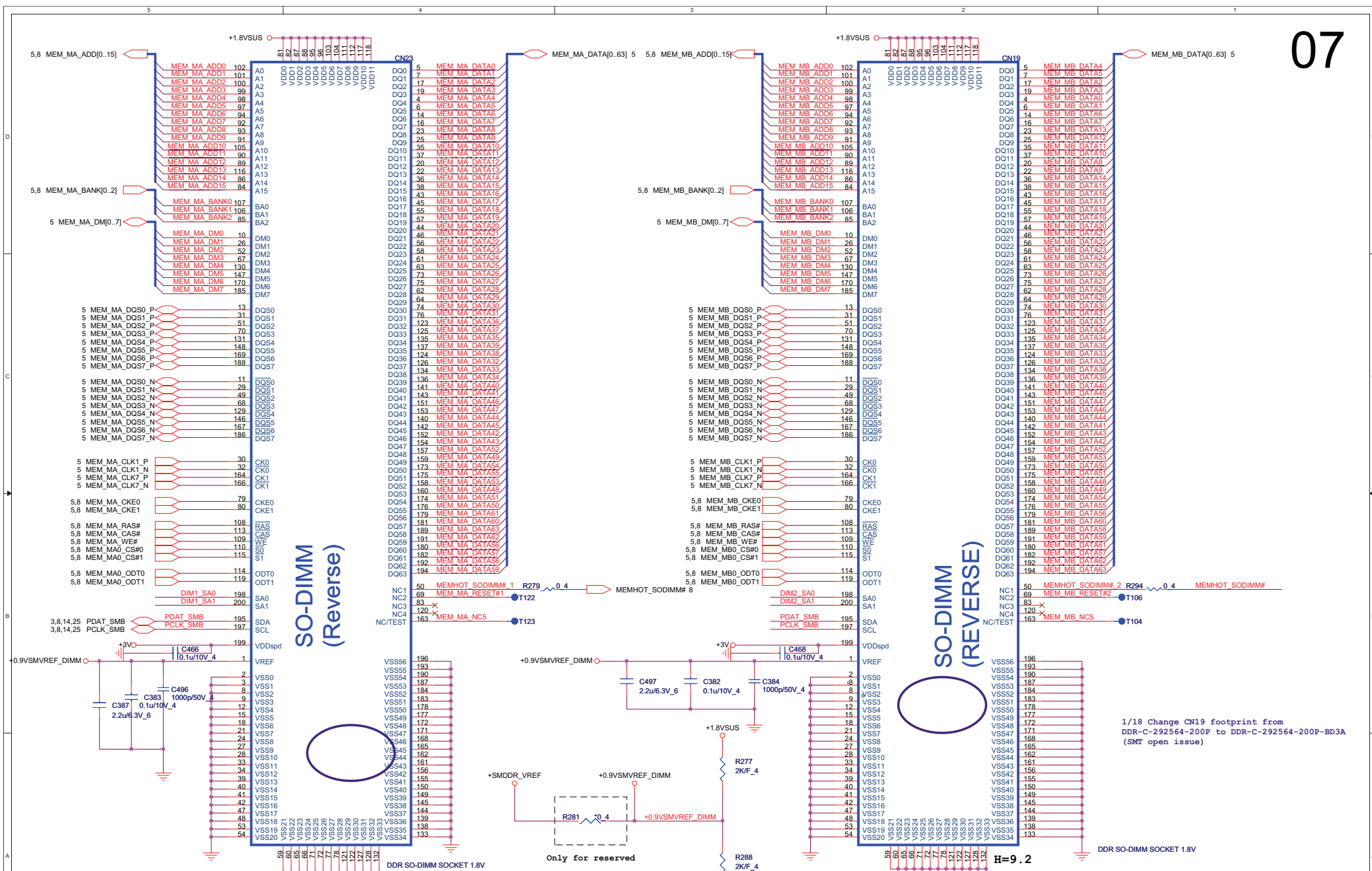


PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	S1G2 DDRII MEMORY I/F 2/3	1A
Date:	Thursday, May 29, 2008	Sheet 5 of 42

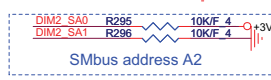
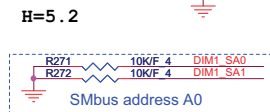


PROCESSOR POWER AND GROUND



SO-DIMM (Reverse)

SO-DIMM (REVERSE)



1/18 Change CN23 footprint from DDR-C-1734071-200P to DDR-C-1734071-200P-BD3A (SMT open issue)

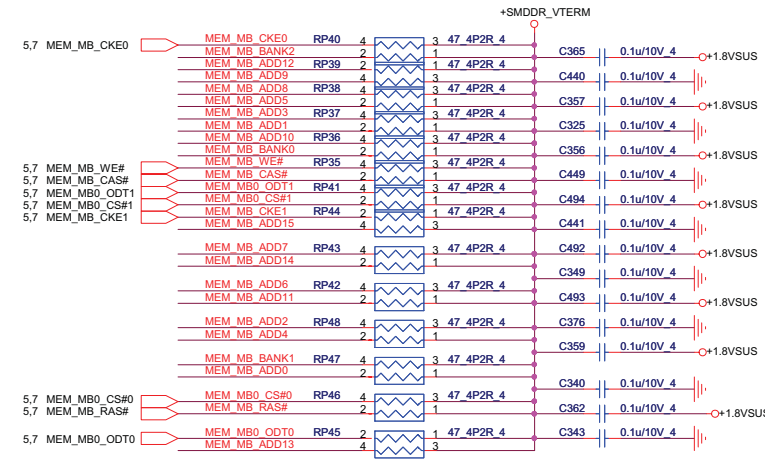
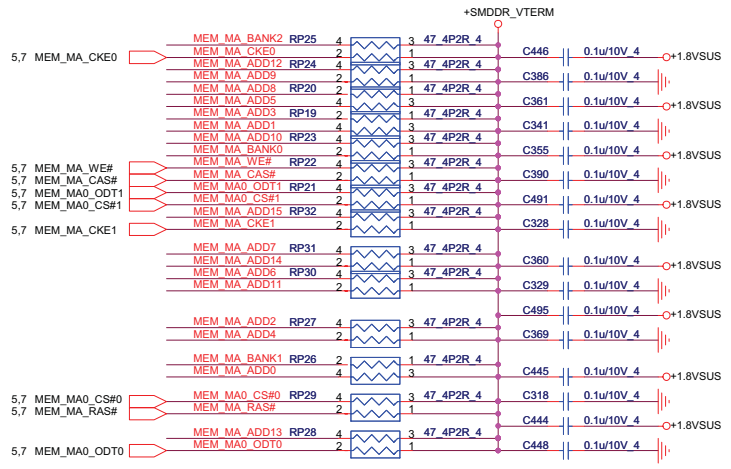
1/18 Change CN19 footprint from DDR-C-292564-200P to DDR-C-292564-200P-BD3A (SMT open issue)

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 SODIMMS: A/B CHANNEL	1A
Date:	Thursday, May 29, 2008	Sheet 7 of 42

5,7 MEM_MA_ADD[0..15] MEM_MA_ADD[0..15]
 5,7 MEM_MA_BANK[0..2] MEM_MA_BANK[0..2]

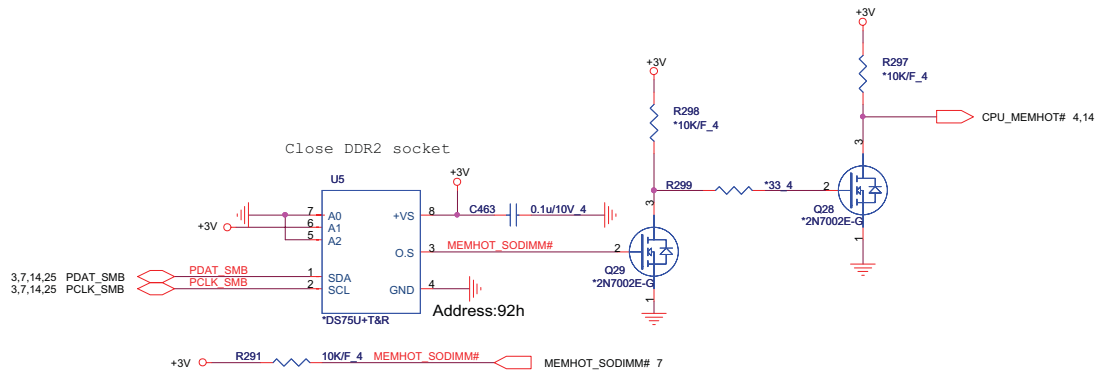
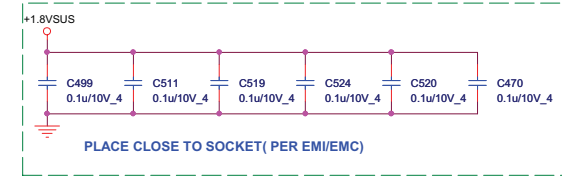
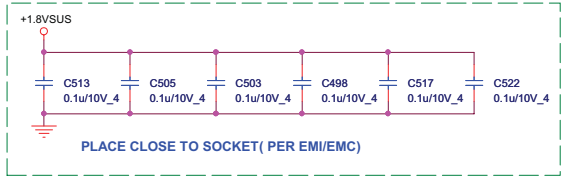
5,7 MEM_MB_ADD[0..15] MEM_MB_ADD[0..15]
 5,7 MEM_MB_BANK[0..2] MEM_MB_BANK[0..2]



PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH





signals	RS780	RX780
HT_TXCALP	R641 300 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 300 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

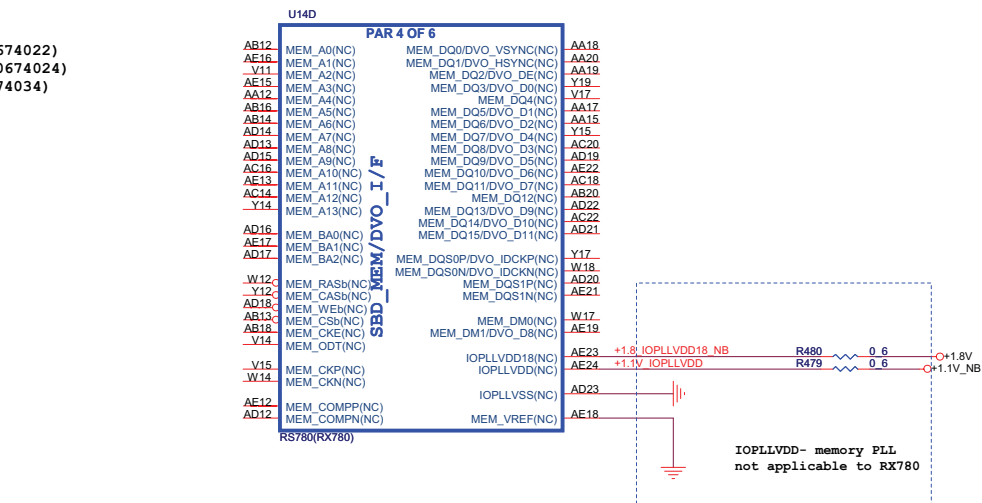
RES CHIP 1.21K 1/16W +-1% (0402)
P/N : CS21212FB18

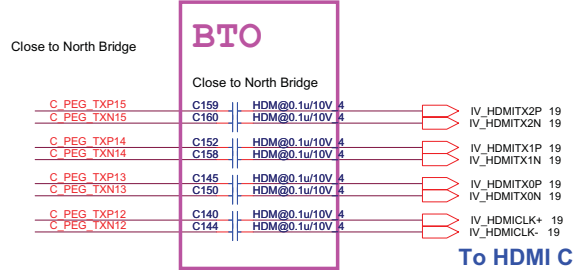
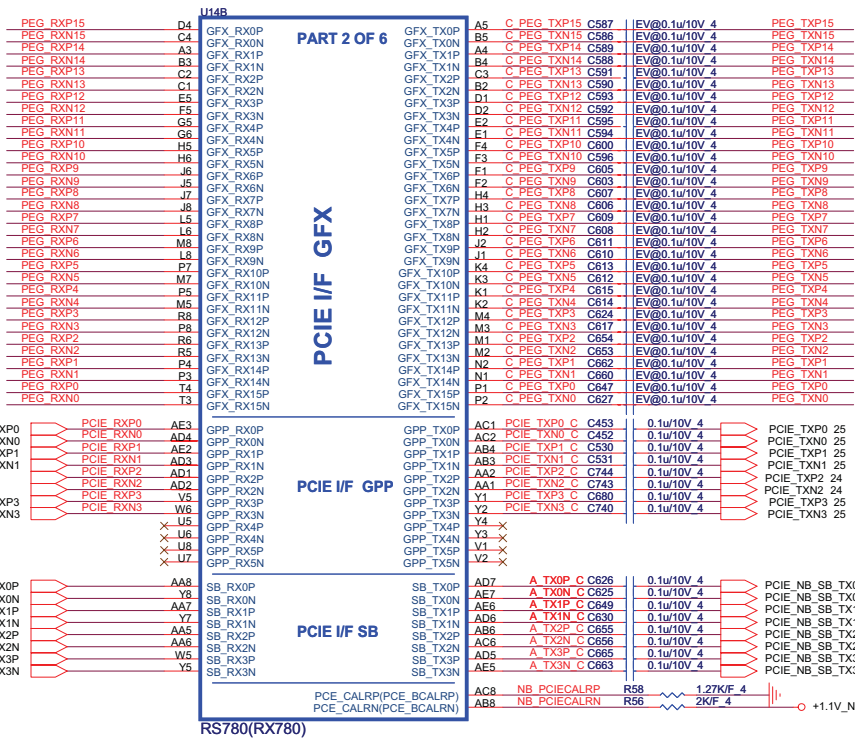
RES CHIP 300 1/16W +-1% (0402)
P/N : CS13002FB00

This block is for UMA RS780 only , RX780 can remove all component

A12 version
RS780M AJ067400T05 100-CK2612 (216-0674008-00)
RS780MC AJ067400T06 100-CK2613 (216-0674010-00)
RX781 AJ067400T10 100-CK2642 (215-0674024)
SB700 AJA12FG0T18 100-CK2614 (218S7EALA12FG)

A13 version
RS780M AJ067400T18 100-CK2699 (216-0674022)
RS780MC AJ067400T20 100-CK2704 (216-0674024)
RX781 AJ067400T21 100-CK2706 (215-0674034)
A12 version
SB700 AJA12FG0T18





- TO WLAN
- TO MINI CARD
- TO PCIE-LAN
- TO EPRESS CARD



NOTE :
RS780MC no support Graphic / HDMI

11/4 modify RX780/RS740/RS780 difference table (PCIE LINK)

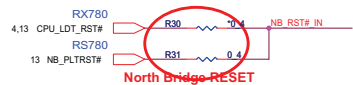
	RS740	RX780/RS780
NB_PCIECALRP	362R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

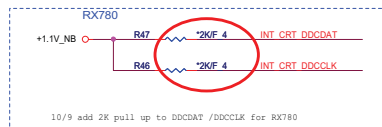
DP0	GFX_TX0, TX1, TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7 AUX1 and HPD1

RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

10/26 change to 4 pin S-video conn, no need TV_comp
2/1 Follow A13 request change R103 from 150 to 140 CS11402FB19



11/4 stuff R5160 for RS780M/MC/RX781



11/4 no stuff for RS780M/MC/RX781

12/22 stuff R48 2.2K for power play



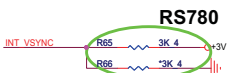
selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EPROM
if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT



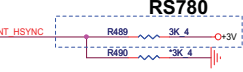
Enables Debug Bus access through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780



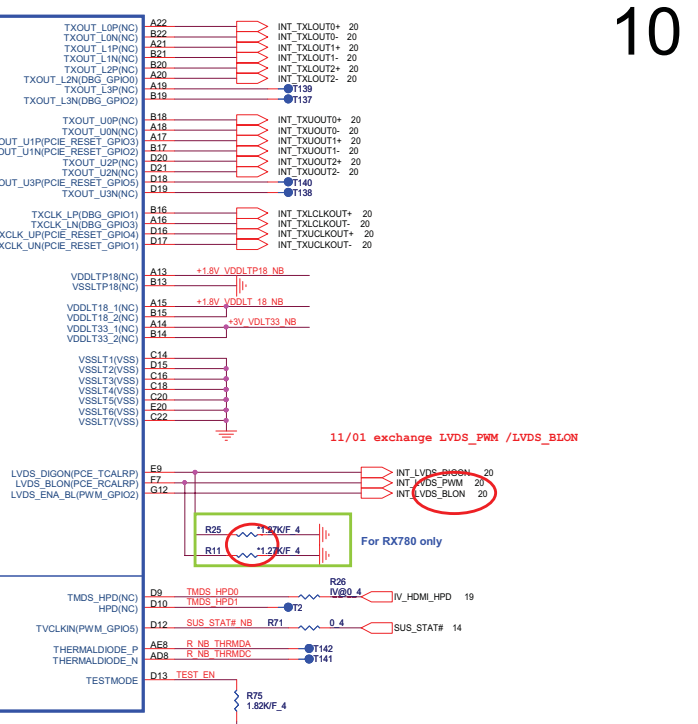
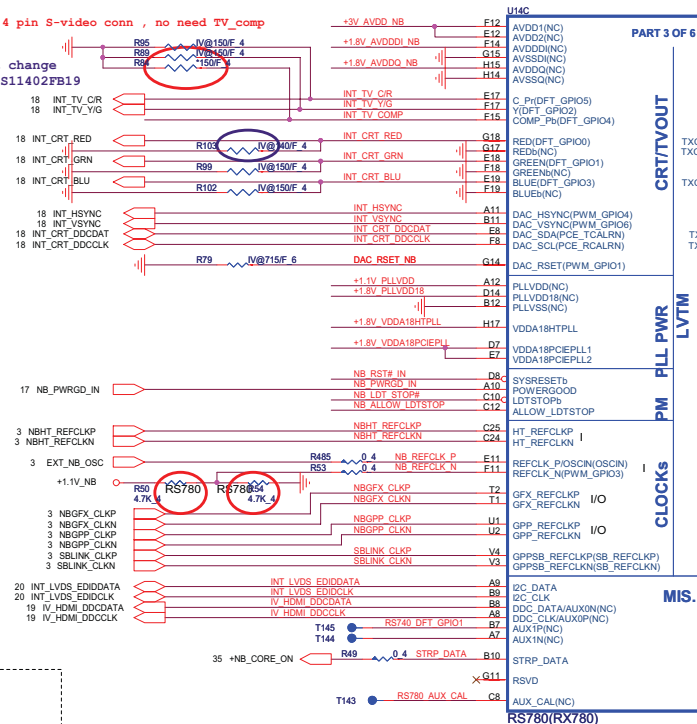
Enables Debug Bus access through memory T/O pads and GPIO.
1 : Enable RS780 , Default
0 : Disable RS780
(RS780 use VSYNC#)



Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)



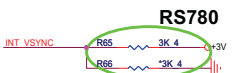
10/19 RS780M Databook rev 1.01 define High disable



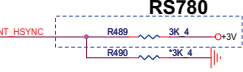
Enables Debug Bus access through memory T/O pads and GPIO.
1 : Enable RX780 , Default
0 : Disable RX780



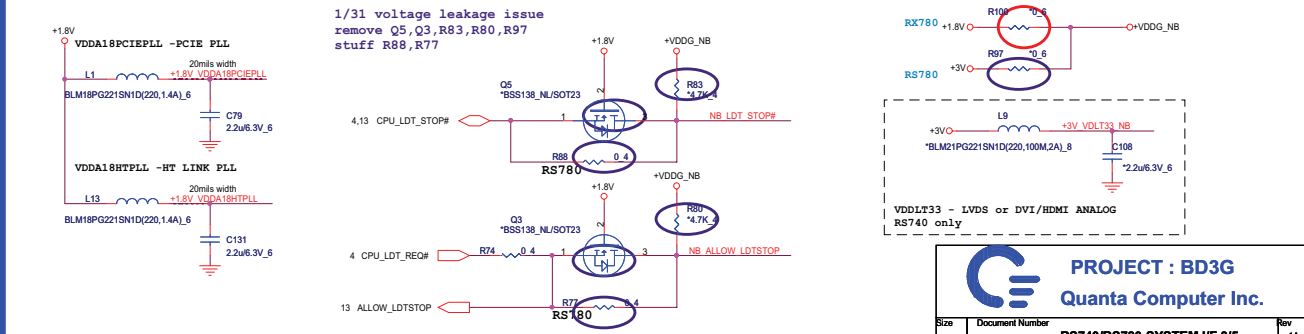
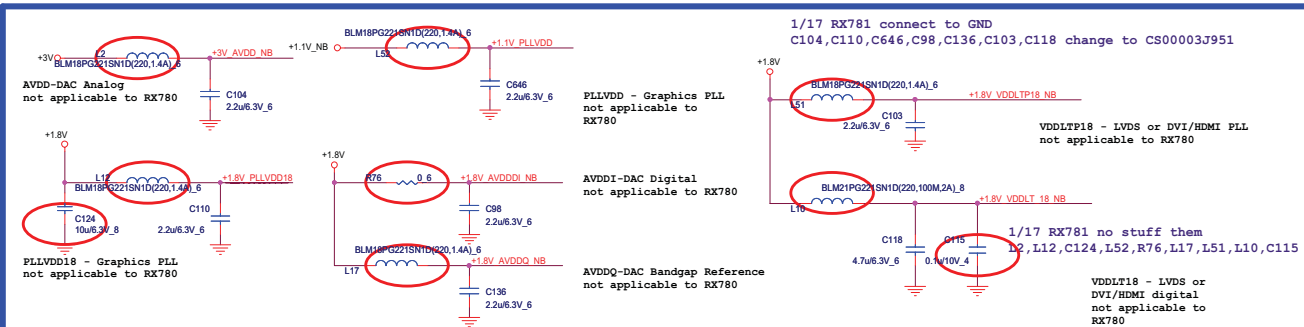
Enables Debug Bus access through memory T/O pads and GPIO.
1 : Enable RS780 , Default
0 : Disable RS780
(RS780 use VSYNC#)



Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)



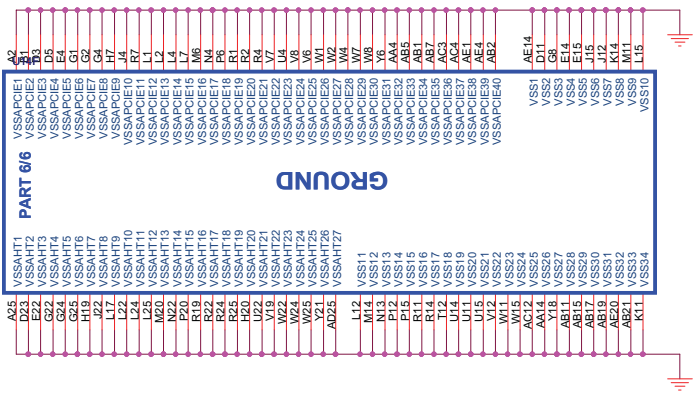
10/19 RS780M Databook rev 1.01 define High disable



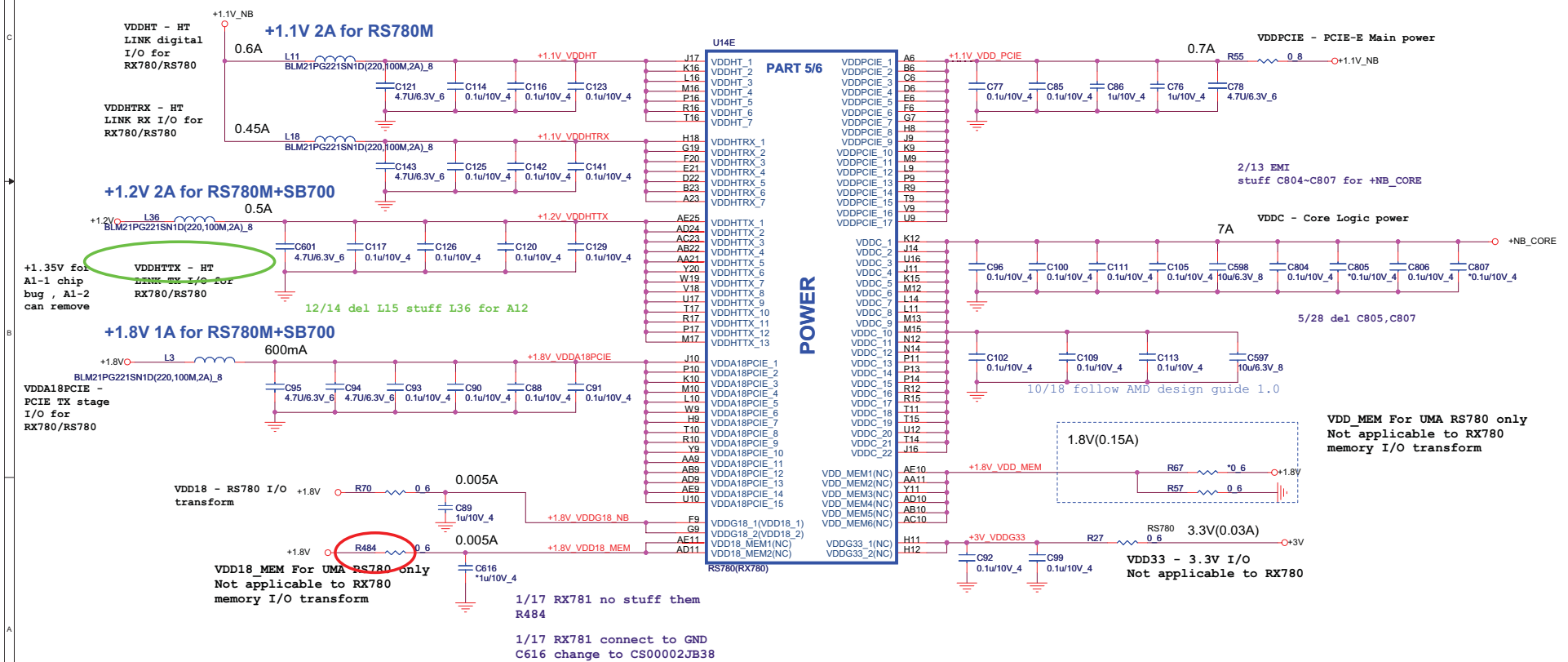
PROJECT : BD3G
Quanta Computer Inc.
RST40/RS780-SYSTEM I/F 3/5
Rev 1A
Date: Thursday, May 28, 2008 Sheet 11 of 42

RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD18	NC	+1.8V	VDDL33	NC	NC



GROUND



PART 5/6

POWER

VDD_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

VDD18_MEM For UMA RS780 Only
Not applicable to RX780
memory I/O transform

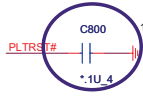
1/17 RX781 no stuff them
R484

1/17 RX781 connect to GND
C616 change to CS00002JB38

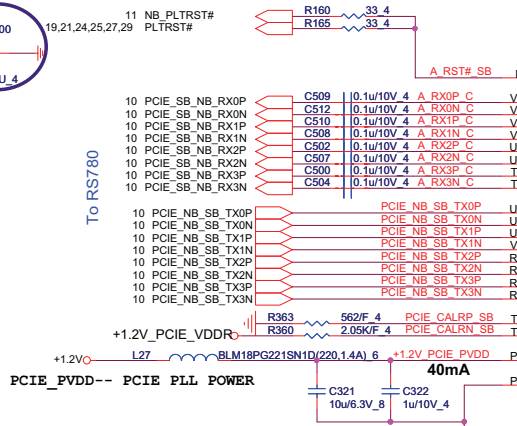
PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	RS740/RS780-POWER5/5	1A
Date:	Thursday, May 29, 2008	Sheet 12 of 42

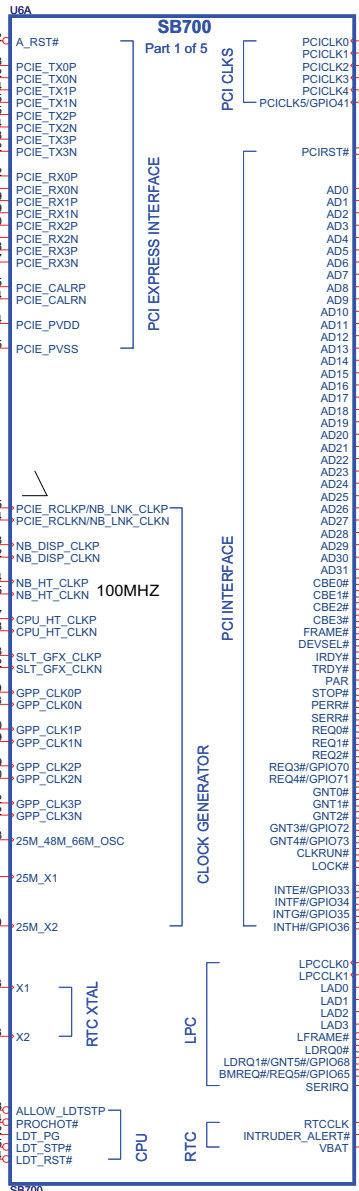
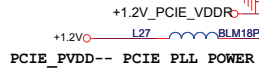
2/4 reserve C800 PLTRST#



PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600



To RS780



PCI EXPRESS INTERFACE

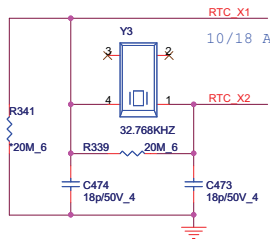
PCI INTERFACE

CLOCK GENERATOR

LPC

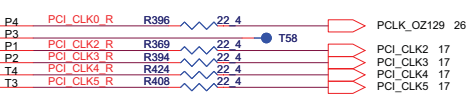
CPU

SB700 IC CTRL (528P) SB700 A11 (218S7EALA11FG) P/N : AJALA110T00

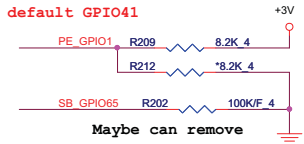


10/18 AMD suggest to not connect to GND

1/31 voltage leakage remove R349



All default PCICLK5 A12 default GPIO41

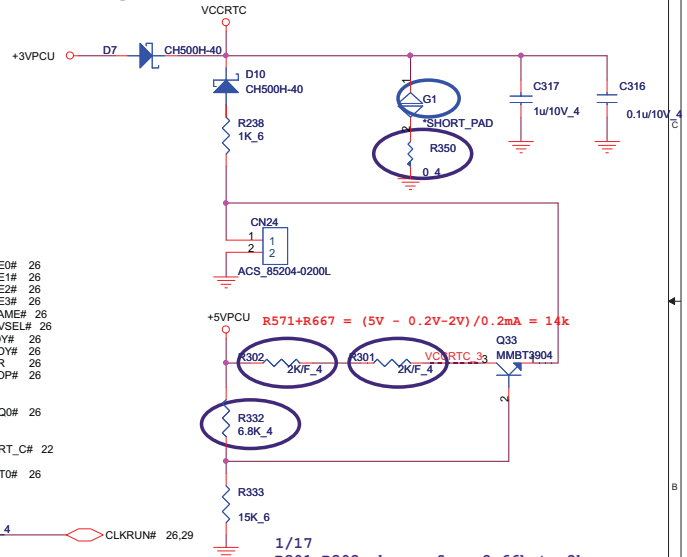


Maybe can remove

All the PCI bus has build-in Pull-UP/Down resistors

4/16 change RTC pad location to G1

RTC



$$R571+R667 = (5V - 0.2V-2V) / 0.2mA = 14k$$

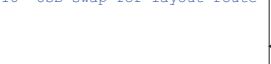
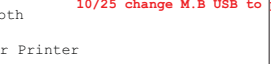
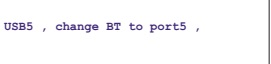
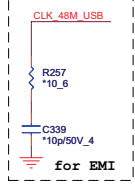
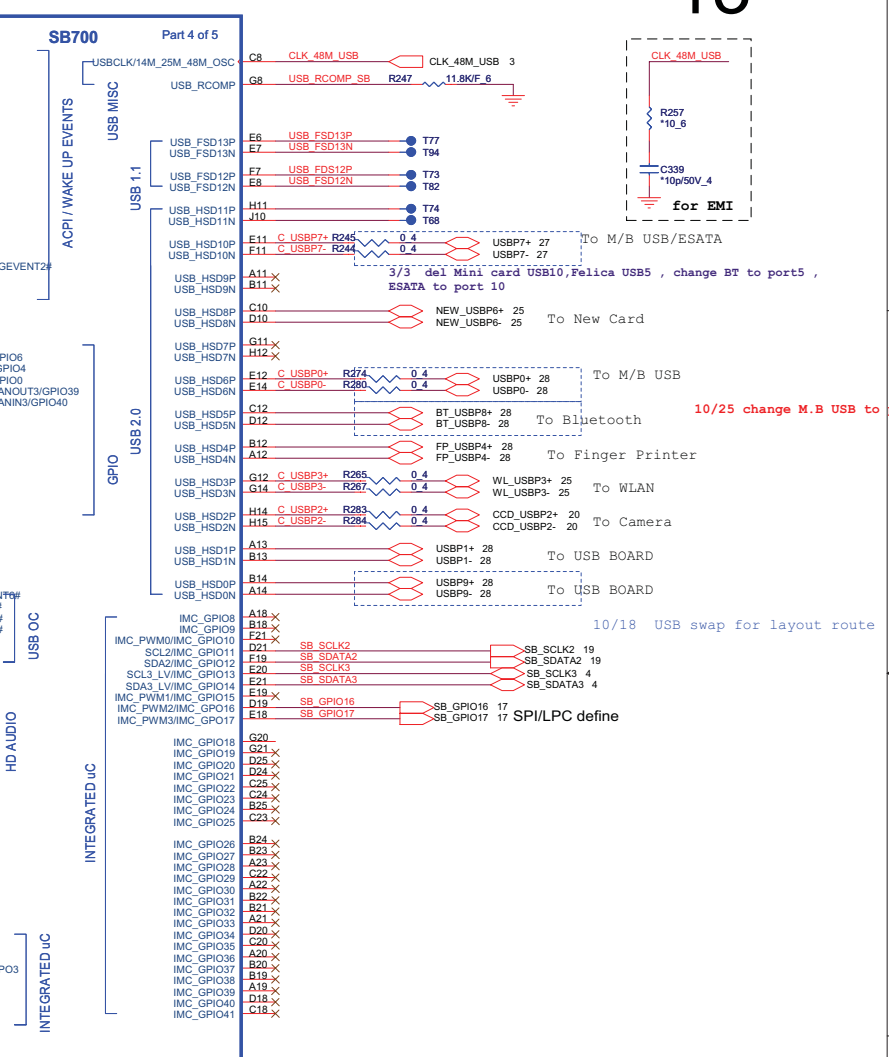
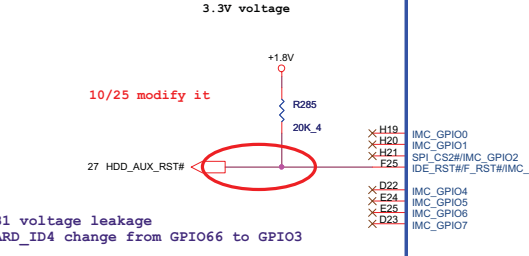
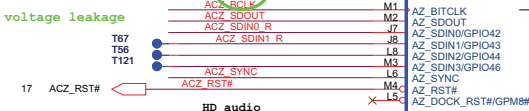
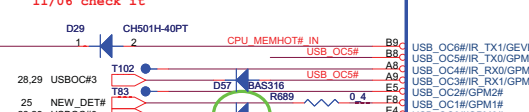
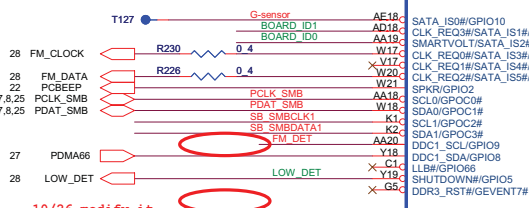
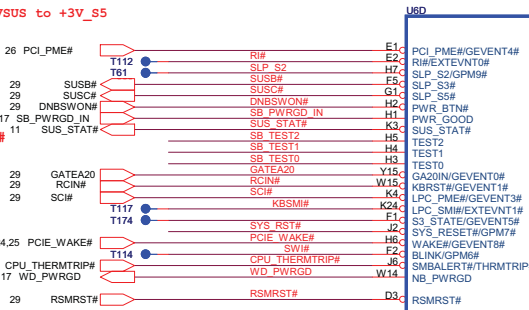
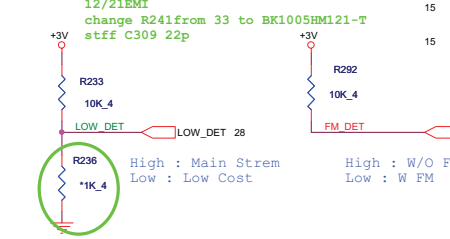
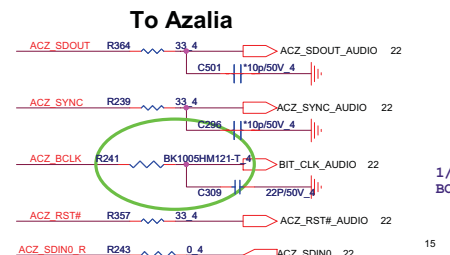
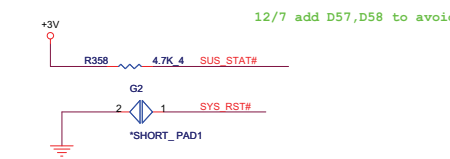
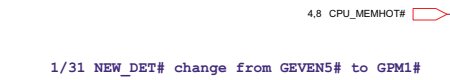
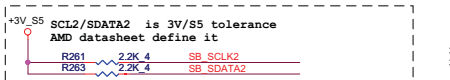
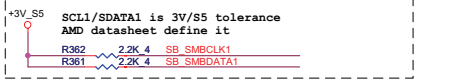
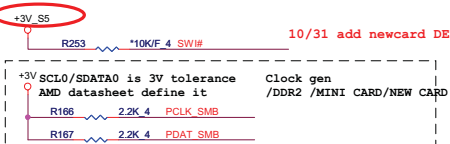
1/17 R301,R302 change from 8.66k to 2k. R332 change from 4.7K to 6.8K

PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	SB700-PCIE/PCI/CPU/LPC 1/4	1A
Date:	Thursday, May 29, 2008	Sheet 13 of 42



11/01 chagne +3VSUS to +3V_S5



MB ID Selection Table

Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD					H
CARD BUS					L
CCFL Panel				H	L
LED Panel				L	L
W/ MXM			H		
W/O MXM			L		
W/ S-VIDEO			H		
W/O S-VIDEO			L		
W/ HDMI			H		
W/O HDMI			L		

1/31 voltage leakage BOARD_ID4 change from GPIO66 to GPIO3

10/25 Board ID define MXM

12/21EMI change R241from 33 to BK1005HM121-T stiff C309 22p

12/4 change PD from 10K to 1K

10/25 change M.B USB to port 6/7

10/18 USB swap for layout route

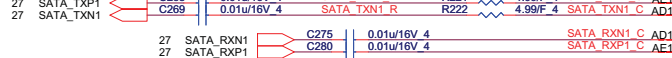
SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB700

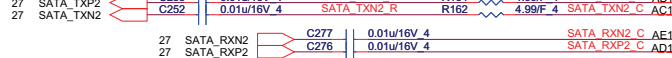
SATA1



SATA2

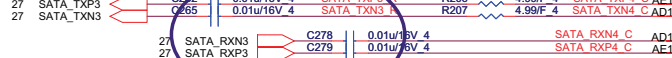


E-SATA



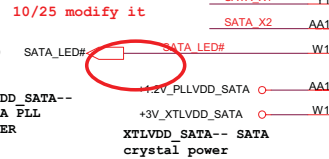
2/22 change SATA ODD from port3 to port4 (solve ODD post detect fail)

ODD

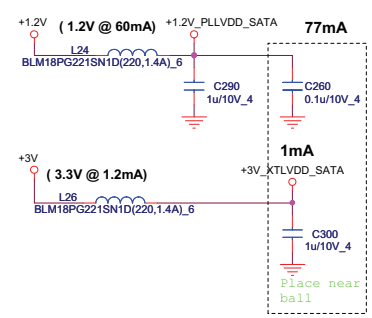
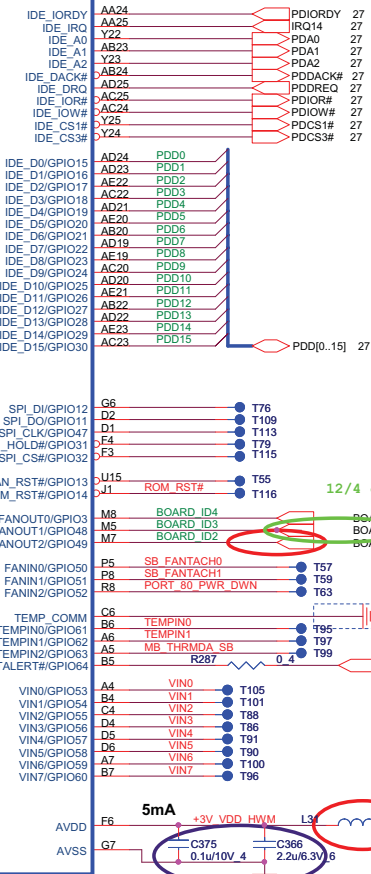
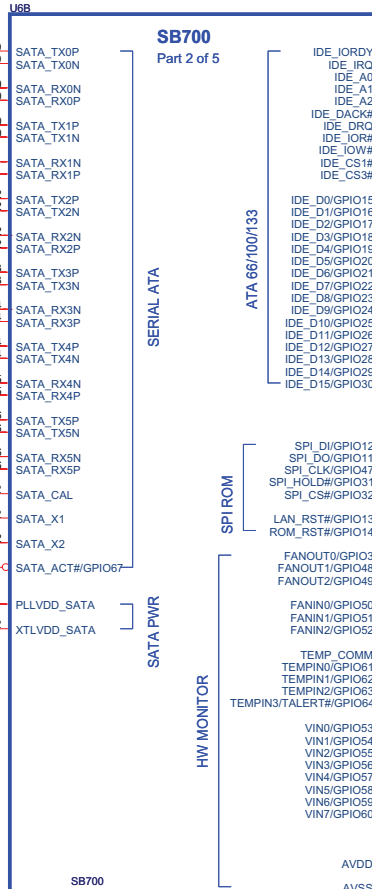
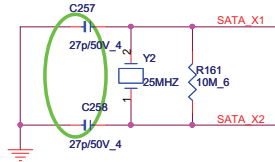


SATA PORT 4,5 are only support IDE mode

NOTE: R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK



12/8 change from 10p to 27p



2/13 EMI stuff C375, C366 for SB HW MONITOR

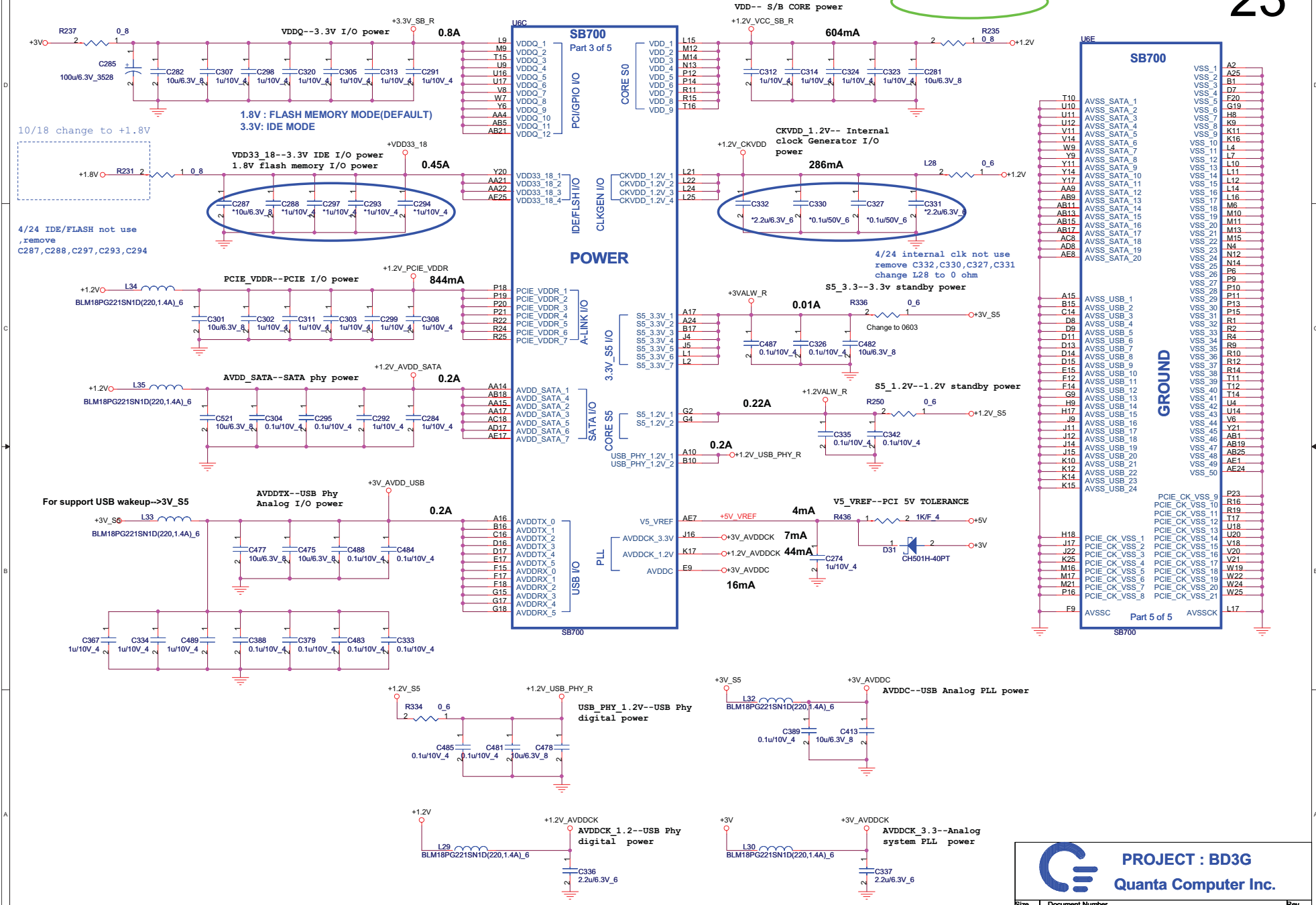
PROJECT : BD3G Quanta Computer Inc. SB700-SATA/IDE/HWM/SPI 3/4


hexaint@hotmail.com

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

12/14 del R234 stuff R235 for A1

23

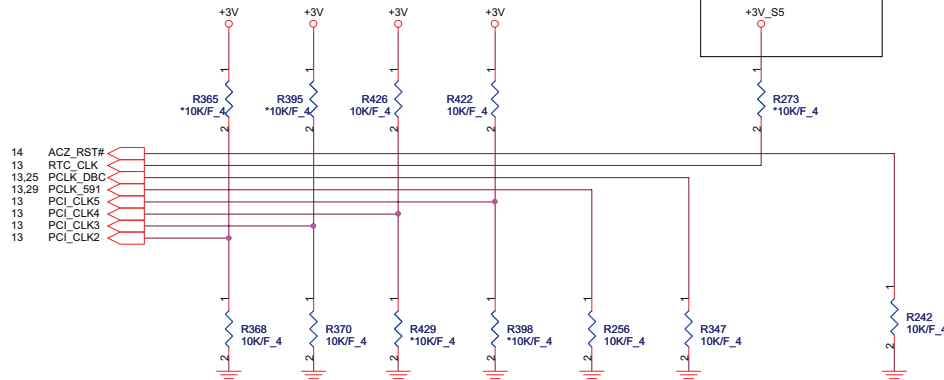


 PROJECT : BD3G Quanta Computer Inc.		Size	Document Number	Rev
			SB700-PWR/DECOUPLING 4/4	1A
Date:	Thursday, May 29, 2008	Sheet	16	of 42



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

It must ready before RSMRST#



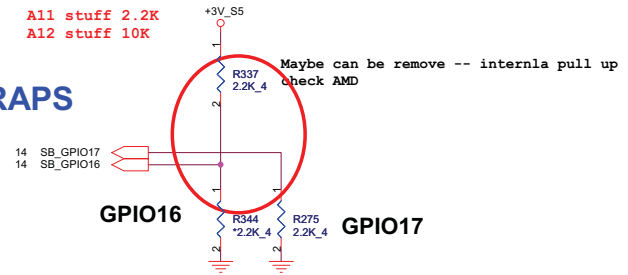
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT_RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

EC ENABLED

ENABLE PCI MEM BOOT

REQUIRED STRAPS

All stuff 2.2K
A12 stuff 10K



Maybe can be remove -- interna pull up check AMD

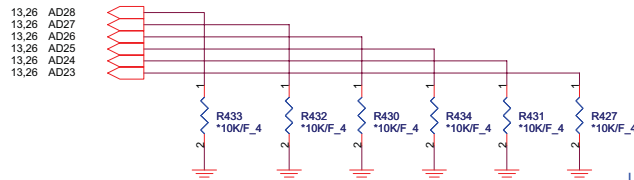
GPIO16 GPIO17

TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

DEBUG STRAPS

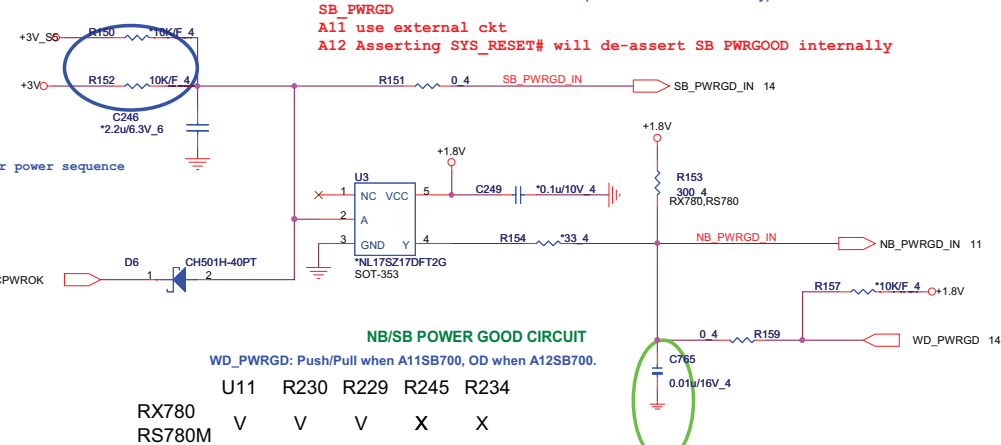
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

4/10 change R150 to R152 for power sequence



SB_PWRGD
All use external ckt
A12 Asserting SYS_RESET# will de-assert SB PWRGOOD internally

NB/SB POWER GOOD CIRCUIT

WD_PWRGD: Push/Pull when A11SB700, OD when A12SB700.

U11 R230 R229 R245 R234

RX780 V V V X X
RS780M

AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353)

ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)

SOT-353

SOT23-5

12/18 add cap for NB_PWRGD signal

4/24 stuff C765 10nf to meet power sequence

PROJECT : BD3G
Quanta Computer Inc.

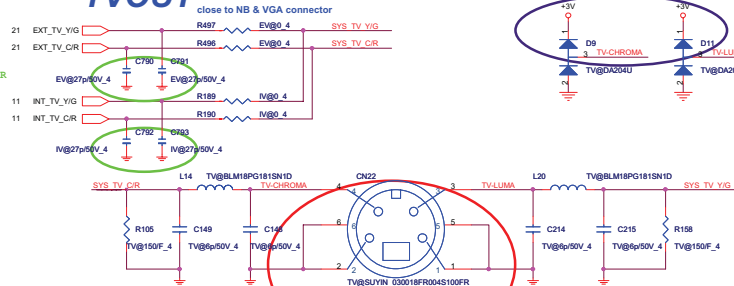
Size	Document Number	Rev
	SB700-STRAPS	1A
Date:	Thursday, May 29, 2008	Sheet 17 of 42

TVOUT BTO

5/8 stuff D9,D11 for S-VIDEO

TVOUT

12/21 EMI
add 27p for TV_Y/G , TV_C/R



10/24 modify it to 4 pin BOI request
10/30 modify footprint to sv-030018FR004S100FR-RVS-4P-H
12/12 update p/n to DFM04FR006
4/16 update footprint to sv-030018fr004s100fr-4p-h-b15m

CRT PORT

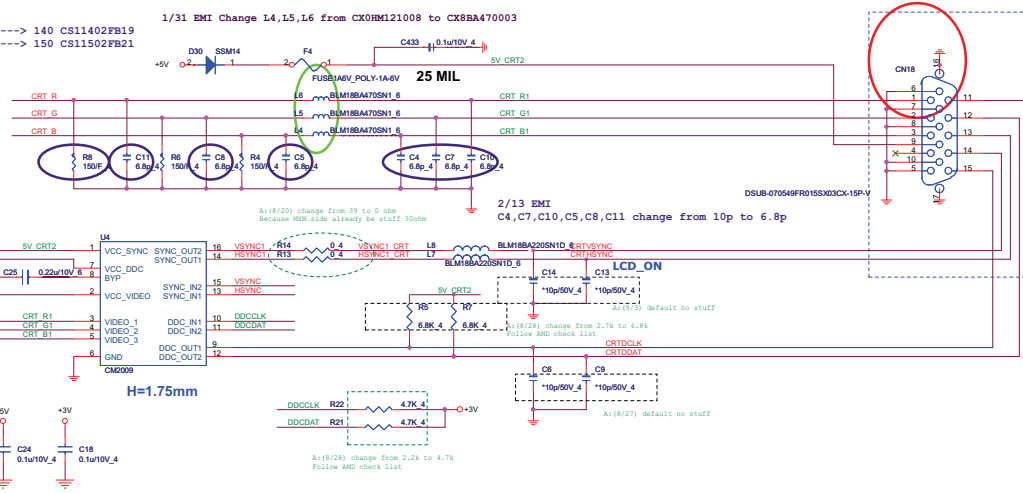
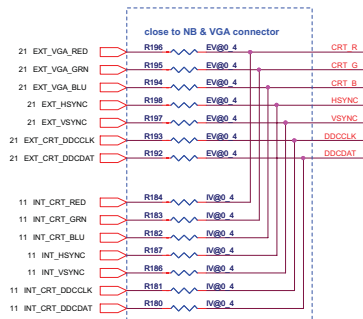
2/1
RS780M A13 R8 ----> 140 CS11402FB19
MXXM R8 ----> 150 CS11502FB21

1/31 EMI Change L4,L5,L6 from CX0HM121008 to CX8BA470003

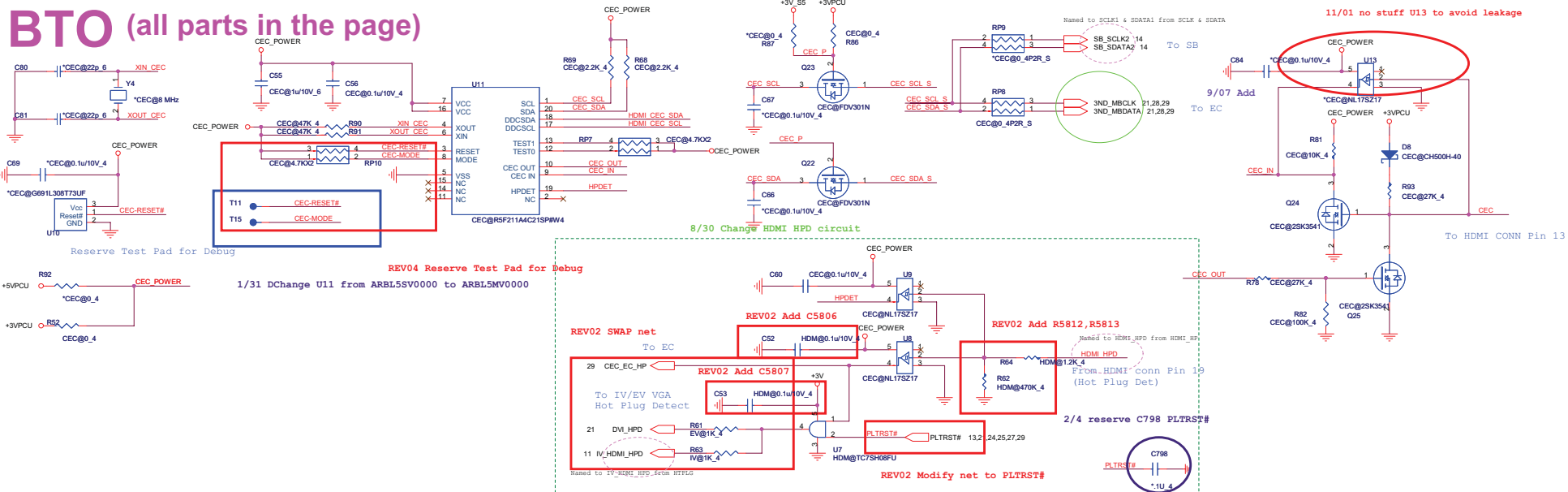
10/12 fix CRT connect error

2/10 DEL D4,D5 footprint and DEL CRT_SENSE# net

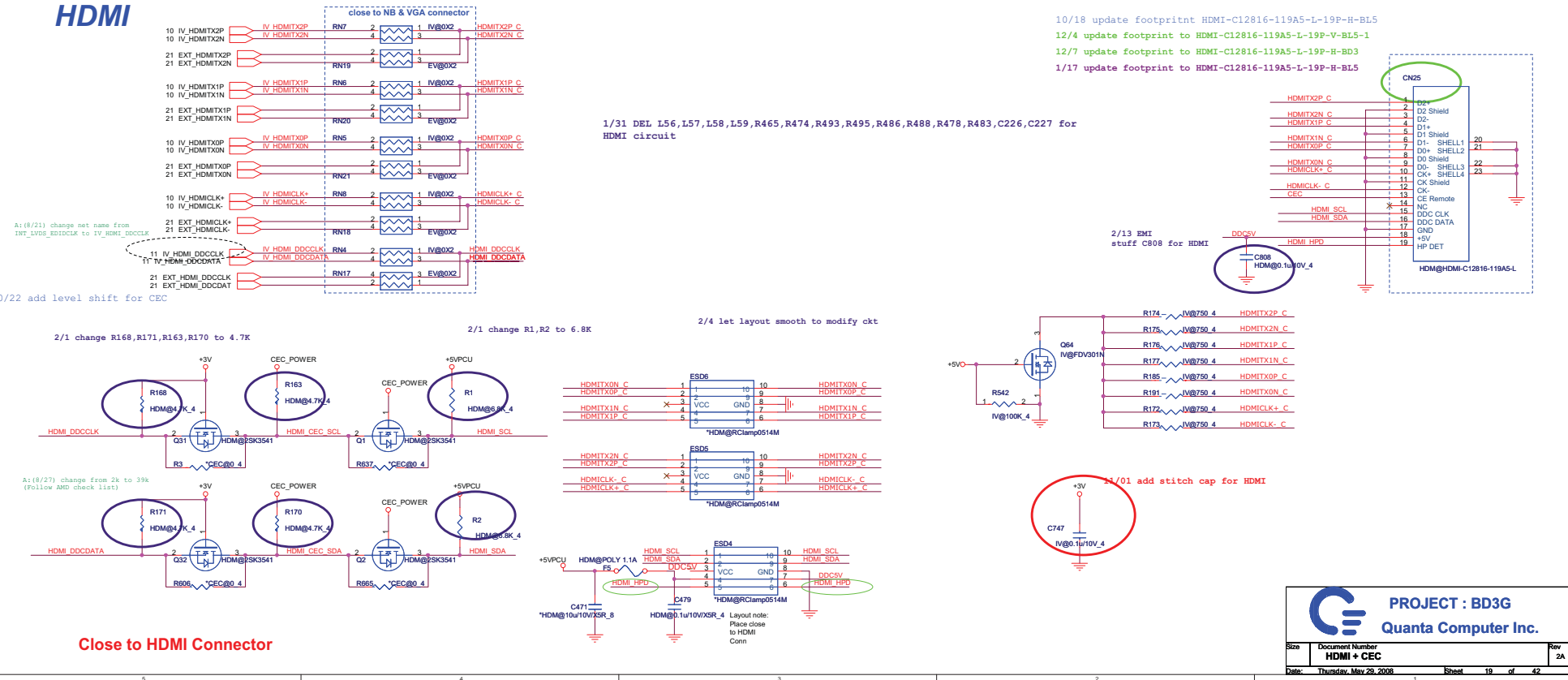
10/25 no use sense



BTO (all parts in the page)

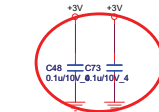
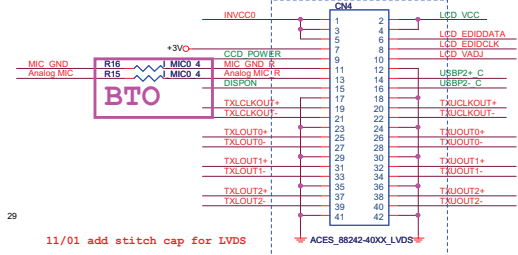
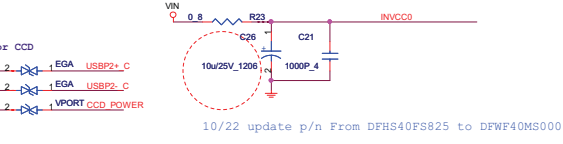
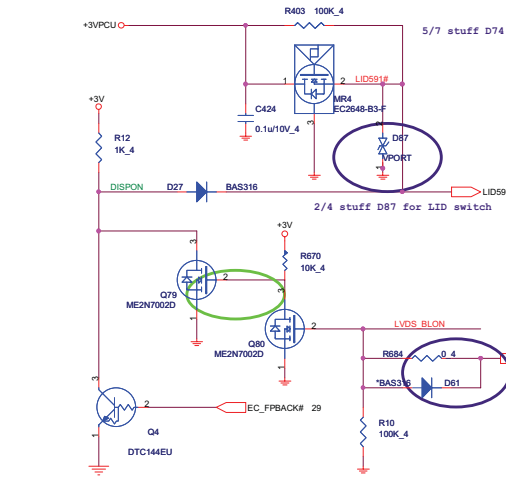
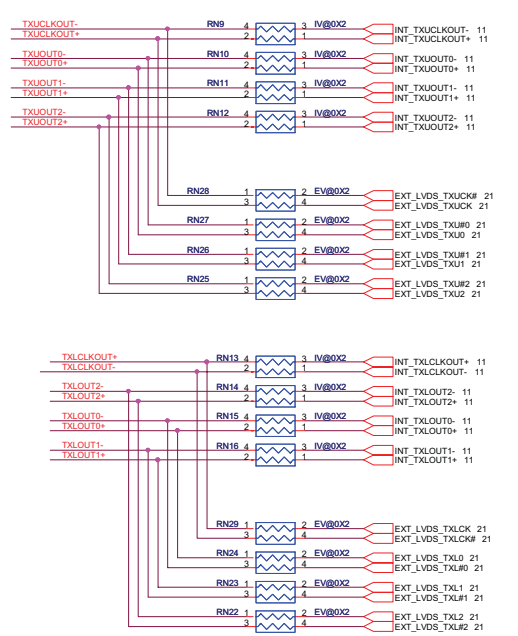


HDMI

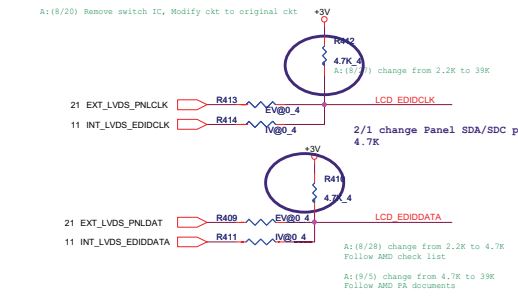
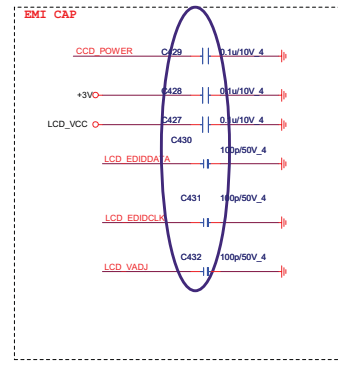
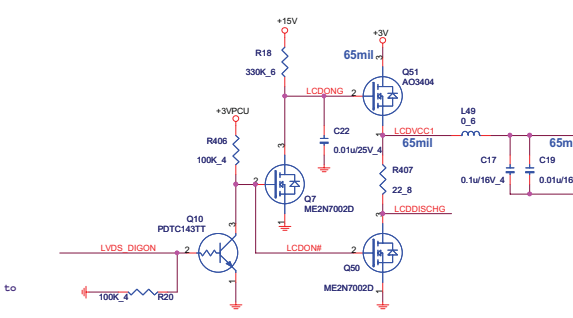


HALL SENSOR

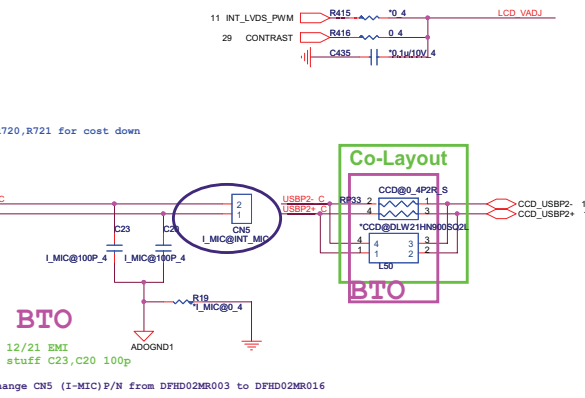
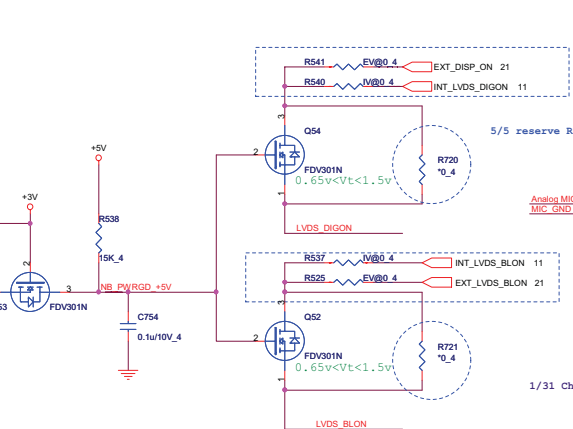
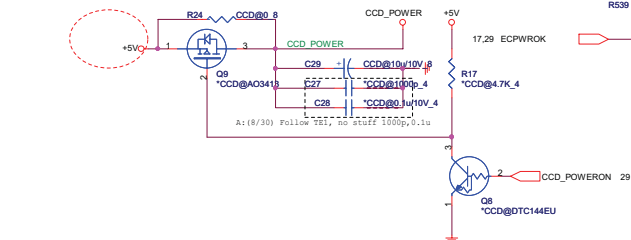
LCD TYPE CONNECTOR



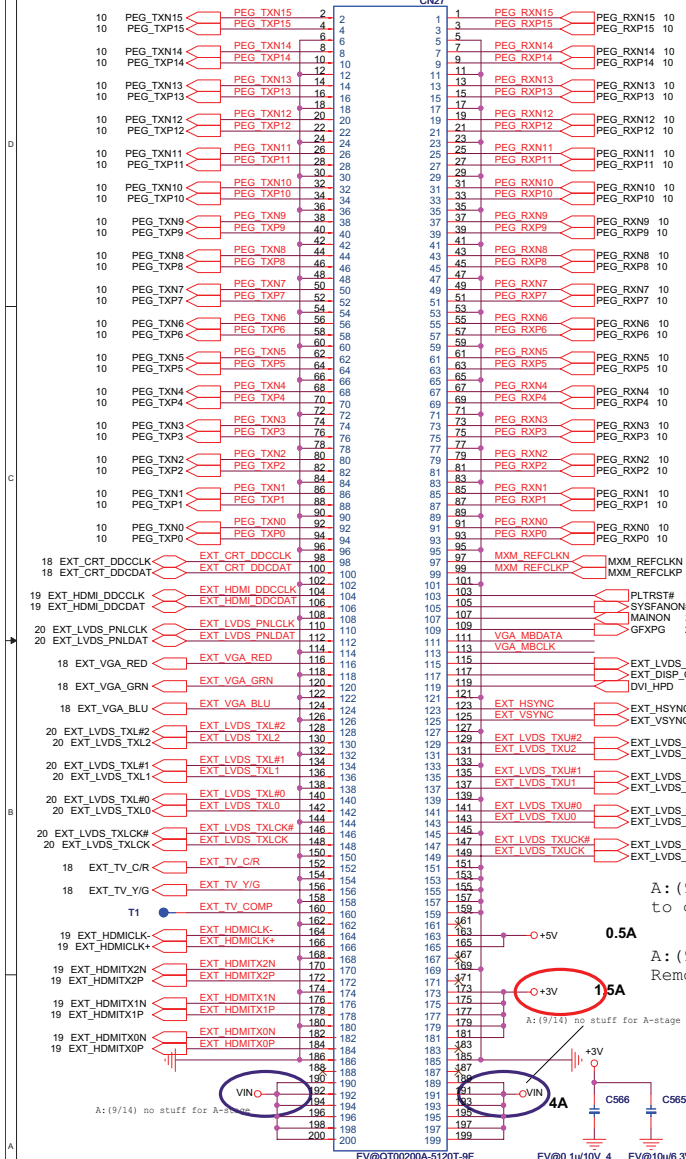
12/4 modify display on ockt to avoid flash when into S3/S4/S5
 1/17 EnergyStar 4.0 Idle power issue
 When BLON= High, Turn ON LCD then turn on MMB
 When BLON= Low, Turn OFF LCD then turn OFF MMB



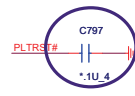
BTO CAMERA MODULE



A: (8/27) Camera module power +5V or +3V?



2/4 reserve C797 PLTRST#

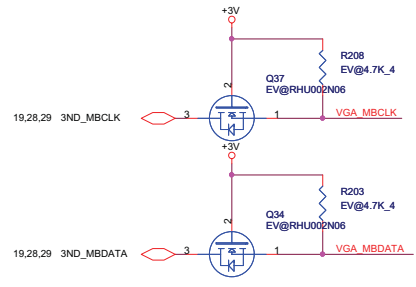


A:(9/18) don't connect pin 161, 167, 171, 183, 187,188 to ground and reserve test point for A build.

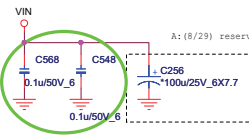
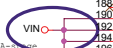
A:(9/19) don't have enough space to put the test point, Remove it for A-test

10/30 modify to +3V

A:(8/29) reserve 100u for VIN




A:(9/14) no stuff for A-build



1/17 Remove R492,R517, Short CN27/Pin189,190 to VIN directly.

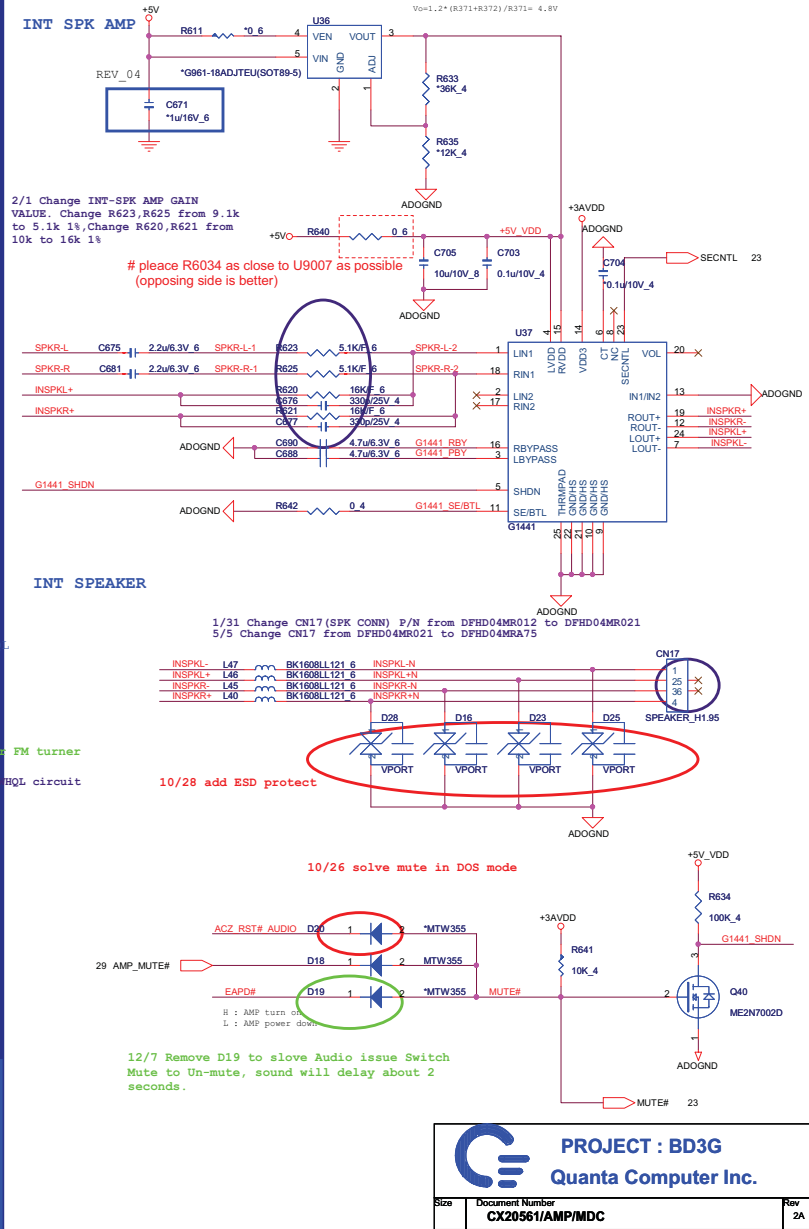
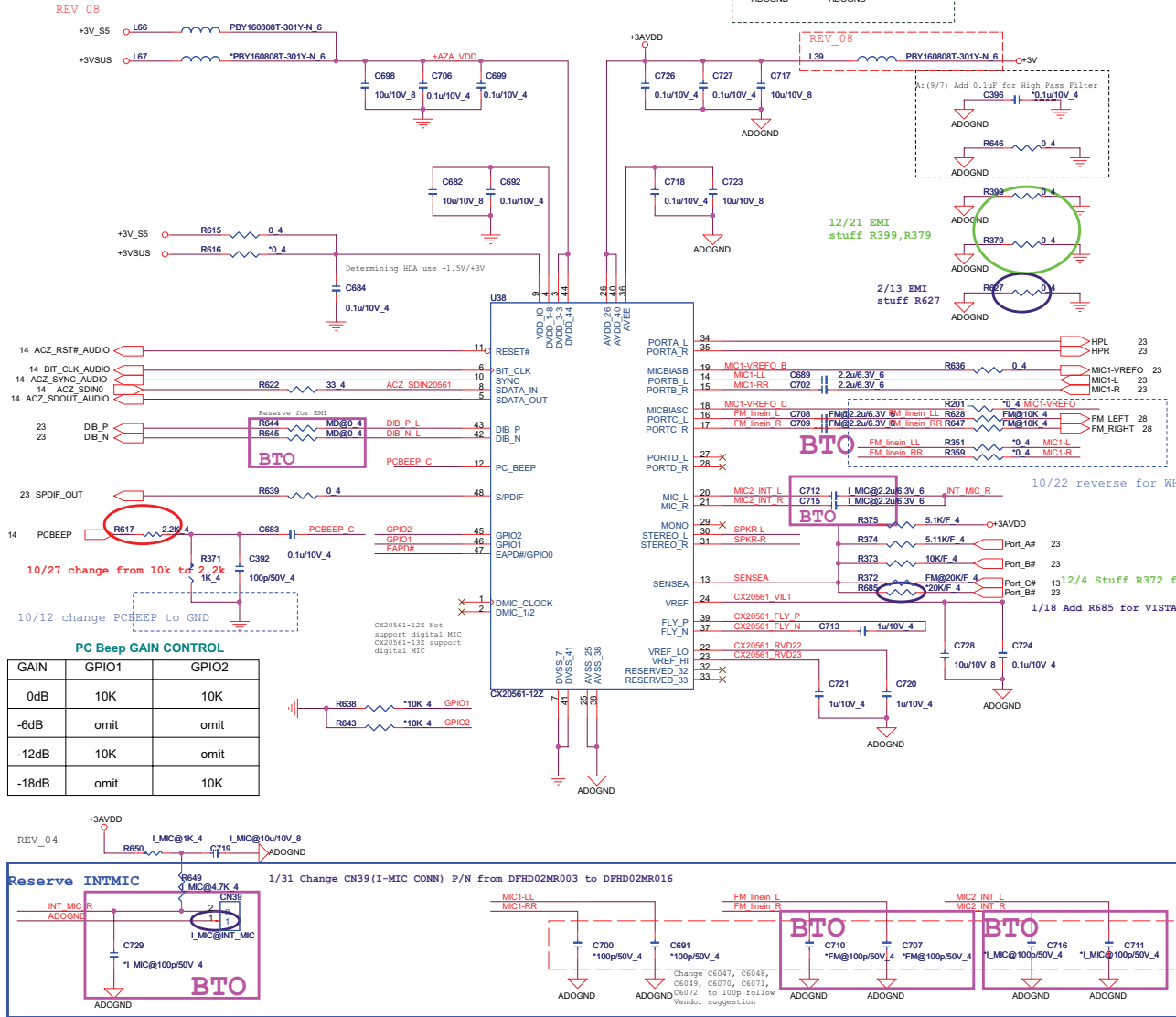
12/21 EMI stuff C568,C548



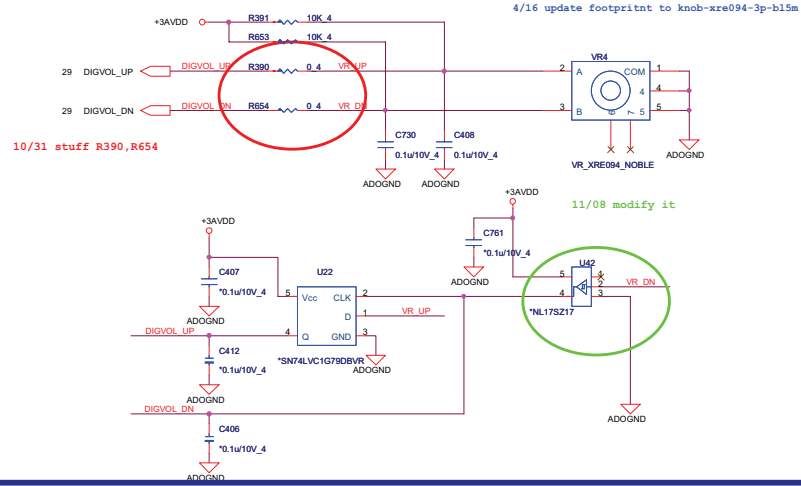
PROJECT : BD3G
Quanta Computer Inc.

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MXM CONNECTOR / TV		2A
Date: Thursday, May 29, 2008		
Sheet 21 of 42		

Codec (CX20561)



VR

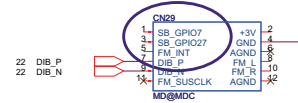


MDC

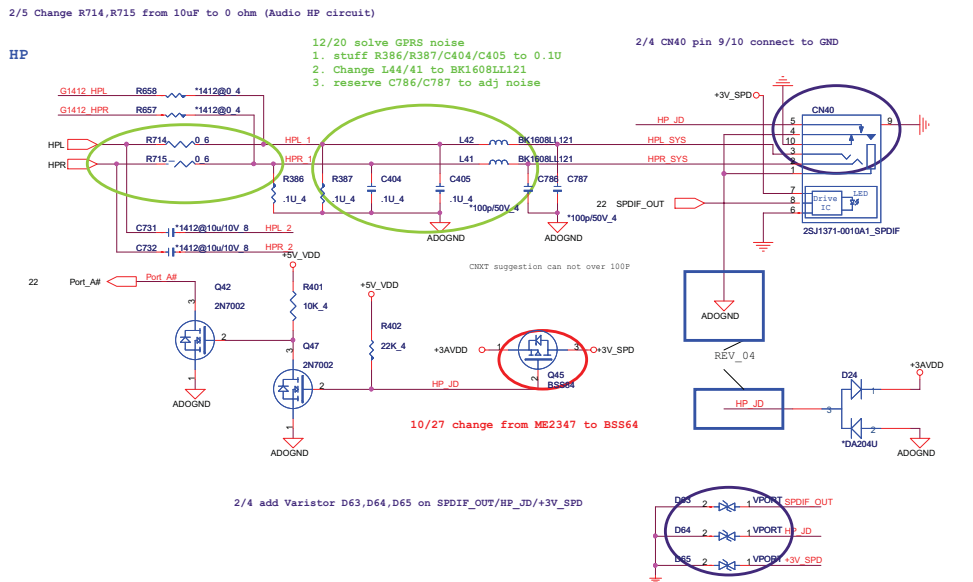
REV_04

1/18 Change CN43 footprint from MDC-1-179373-2-12P-RUV to MDC-1-179373-2-12P-RUV-BD3A (SMT open issue)

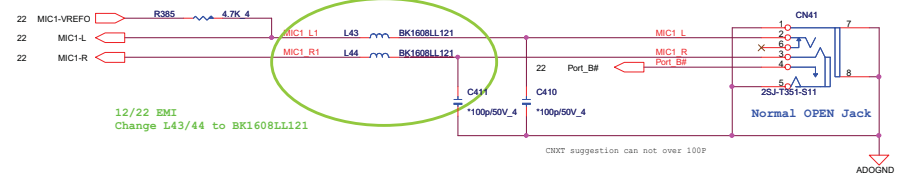
BTO



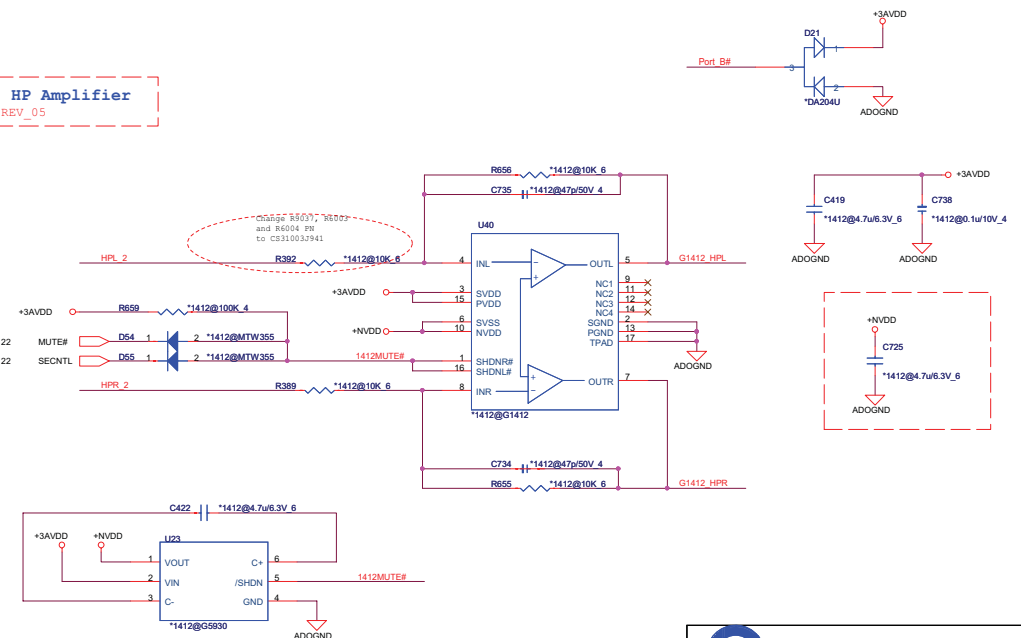
HP



SYSTEM MIC



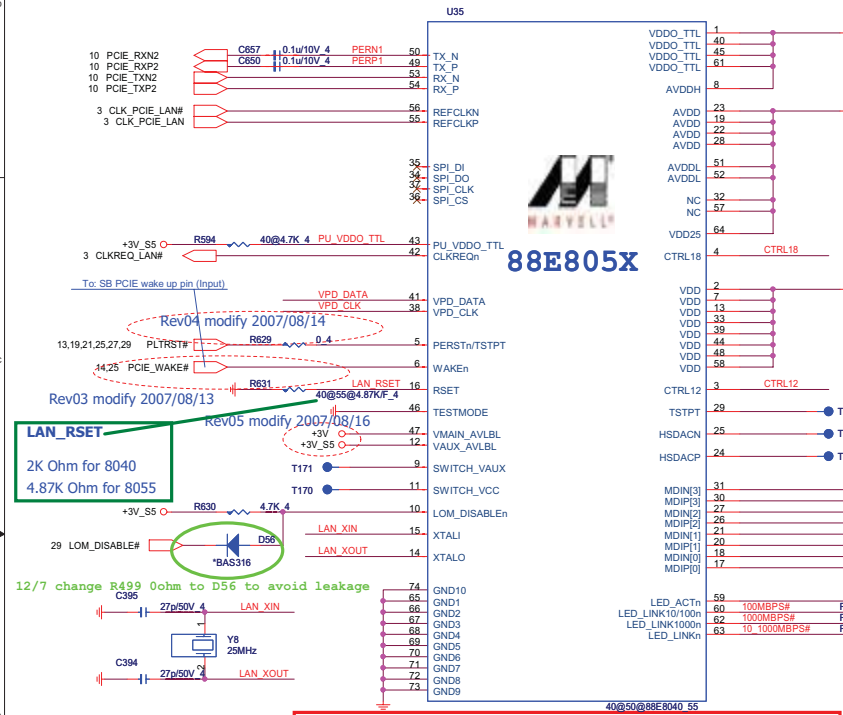
HP Amplifier
REV_05



hexainf@hotmail.com

LAN_MARVELL_88E8040/88E8055

10/100 : 88E8040T P/N : AL008040001
 GIGA : 88E8072 P/N : AL008072000



LAN_RSET
 2K Ohm for 8040
 4.87K Ohm for 8055

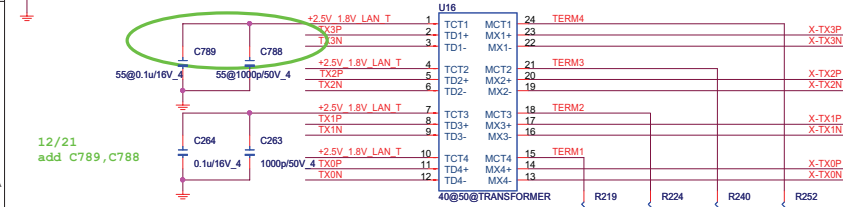
12/7 change R499 0ohm to D56 to avoid leakage

12/21 EMI
 add L74,C766,C767 for +2.5V_1.8V_LAN

DELTA 10/100 : LFE8696-R P/N : DB0MA8LAN00
 H = 4mm GIGA : LFE9291-R P/N : DB0BD3LAN00

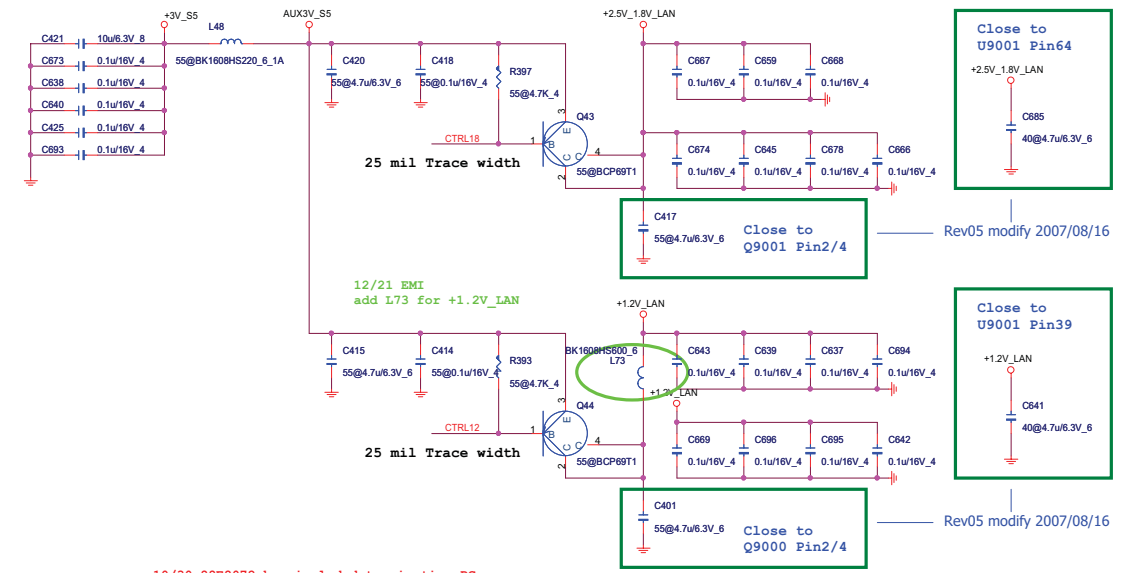
BOTHHAND 10/100 : P/N :
 H = 4mm GIGA : GST5006 P/N : DB0BD3LAN01

HAN WEI 10/100 : HPL-9060 P/N : DBBL5MLAN00
 H = 4mm GIGA : HPL-68 P/N : DB0Z03LAN00



C288
 1000p/3KV_1808
 Check by Safety

Rev05 modify 2007/08/16



Close to U9001 Pin64
 +2.5V_1.8V_LAN
 C885
 40@4.7u6.3V_6

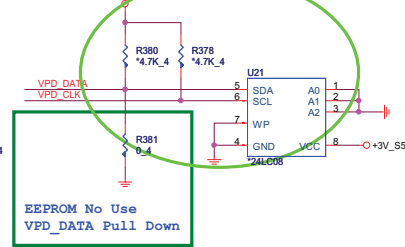
Close to Q9001 Pin2/4
 C417
 55@4.7u6.3V_6

Close to U9001 Pin39
 +1.2V_LAN
 C841
 40@4.7u6.3V_6

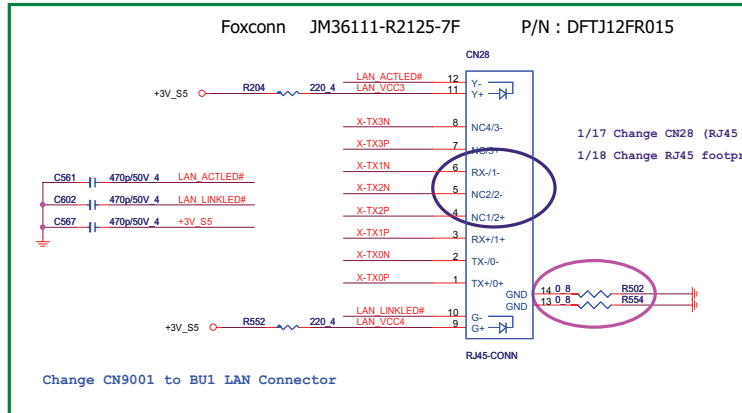
Close to Q9000 Pin2/4
 C401
 55@4.7u6.3V_6

10/30 88E8072 has included termination RC

12/22 cost down remove LAN eeprom stuff R381
 remove U21,R380,R378



EEPROM No Use
 VPD_DATA Pull Down



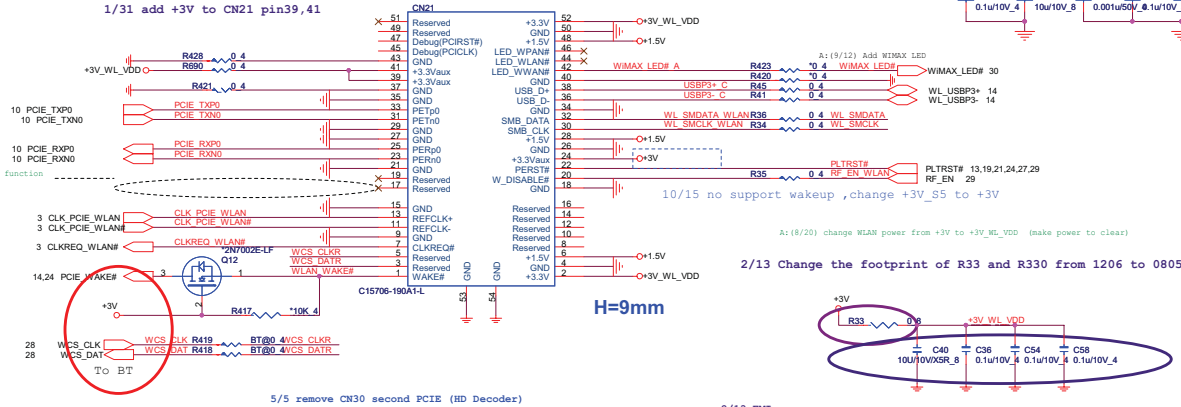
Change CN9001 to BU1 LAN Connector

Rev05 modify 2007/08/16

PROJECT : BD3G
Quanta Computer Inc.

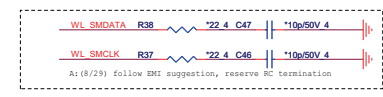
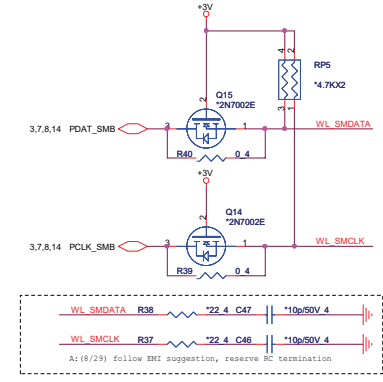
Doc Number: LAN_Marvell_8040/8055
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MINI-Card I (WLAN)

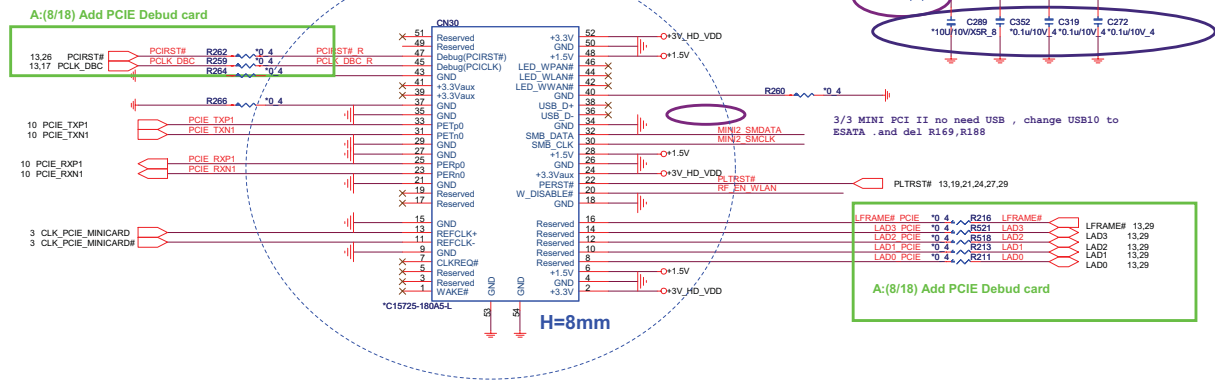


A:(8/18) Due to EC assign Pin11 to other function
Remove uP_BOOT_CK from EC
A:(8/23) Remove uP_GND from EC

A:(8/20) change WLAN power from +3V to +3V_WL_VDD (make power to clear)



MINI-Card II (HD Decoder)

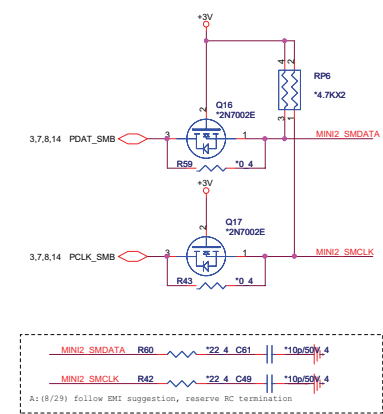


A:(8/18) Add PCIE Debus card

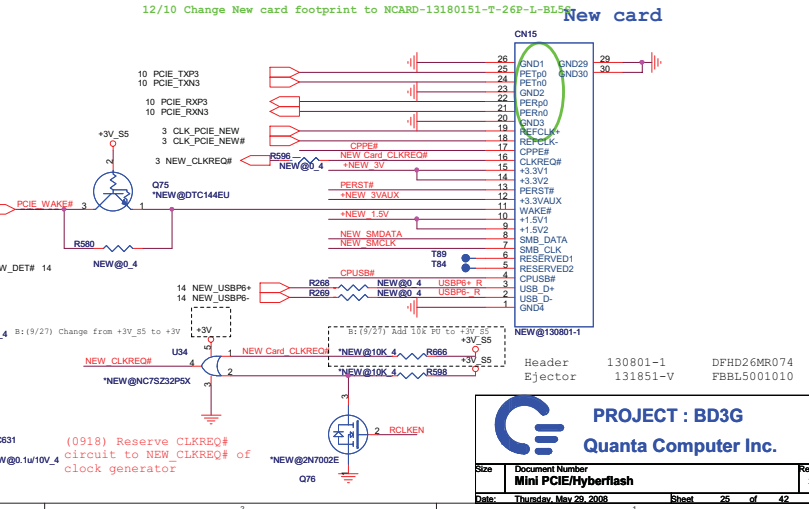
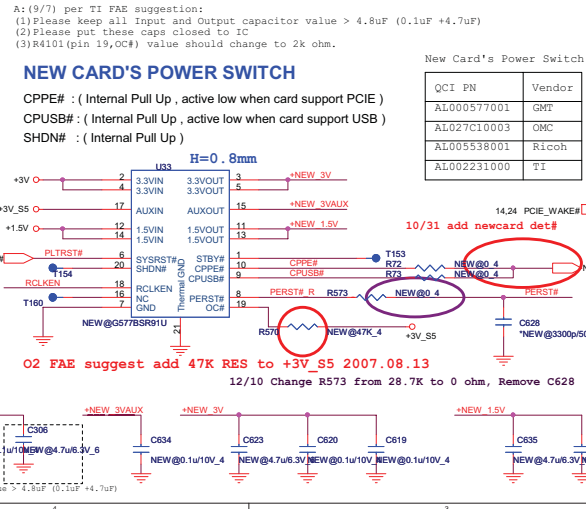
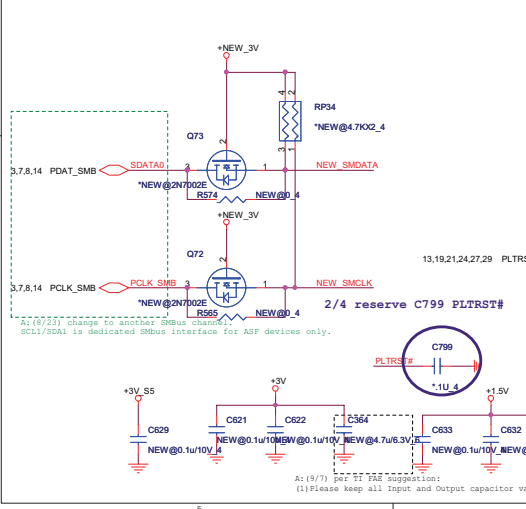
2/13 EMI stuff C40, C36, C54, C58, C289, C352, C319, C272

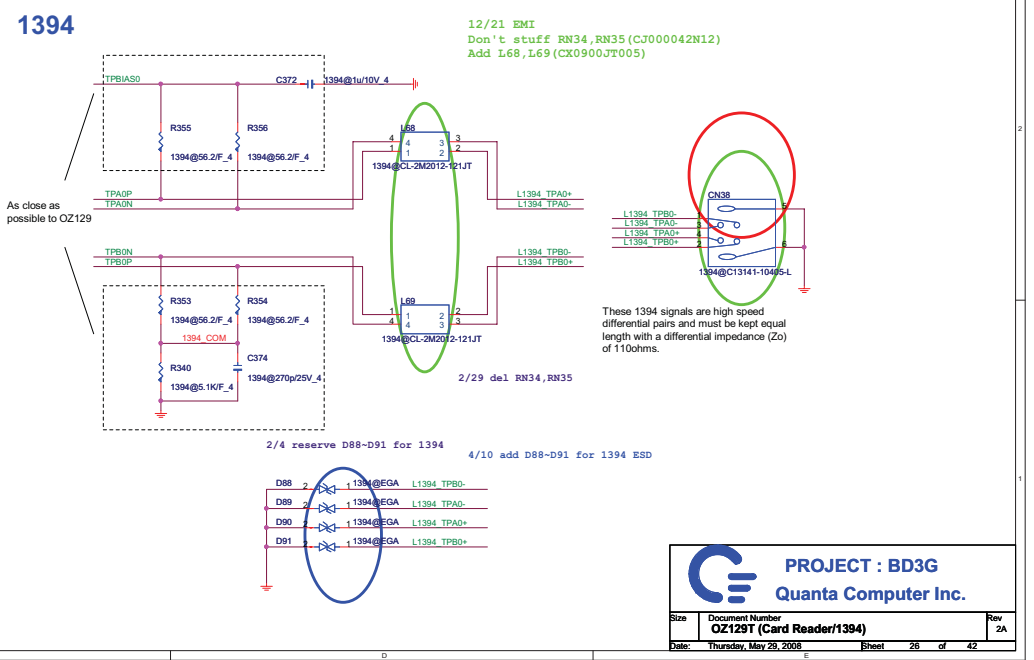
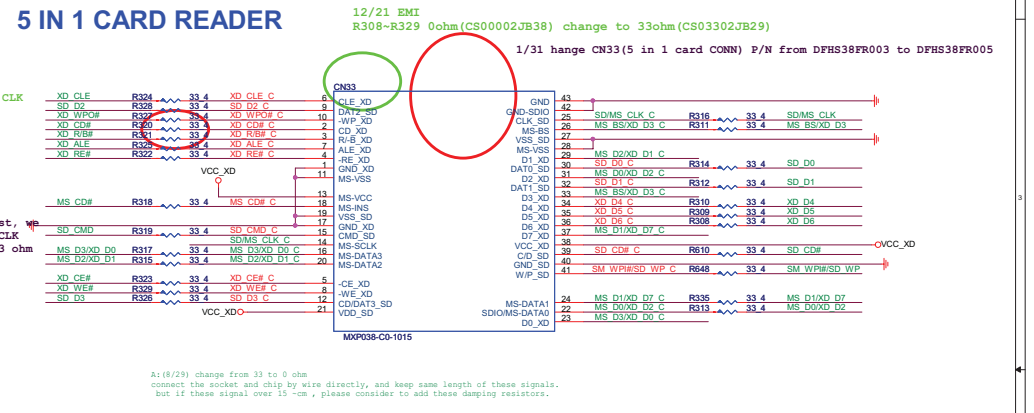
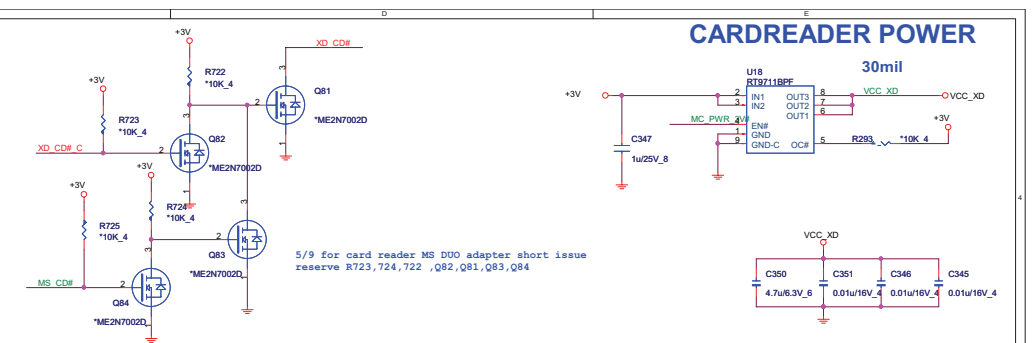
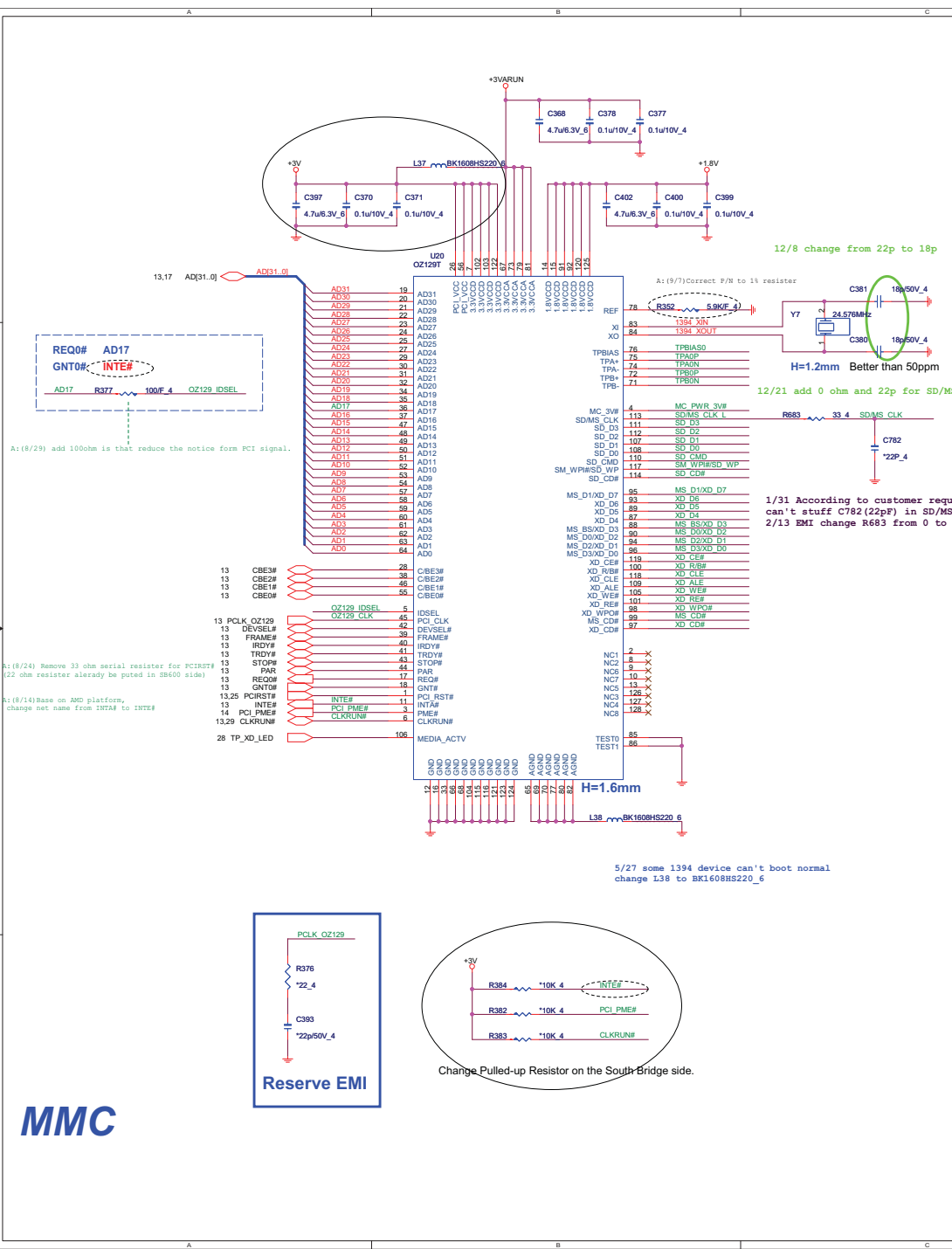
3/3 MINI PCI II no need USB , change USB10 to ESATA .and del R169,R188

A:(8/18) Add PCIE Debus card



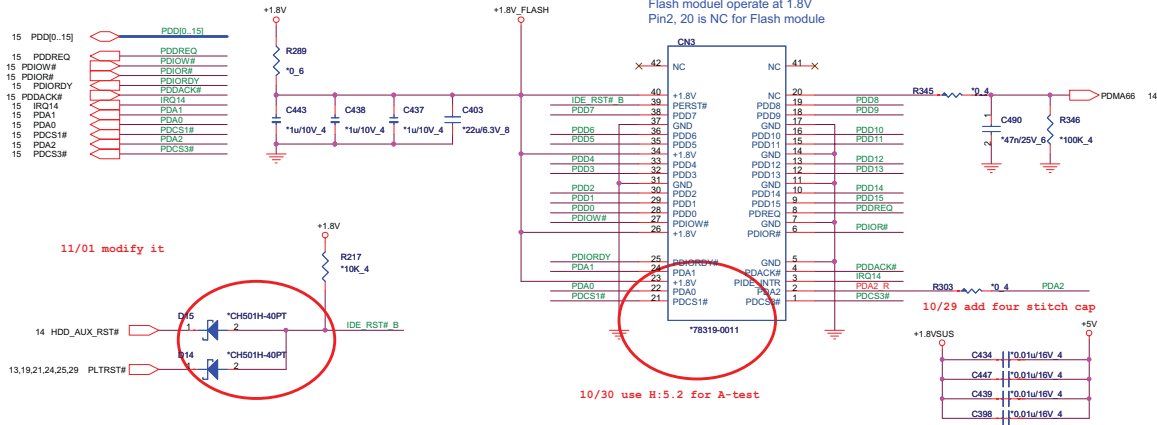
A:(8/29) follow EMI suggestion, reserve RC termination





FLASH

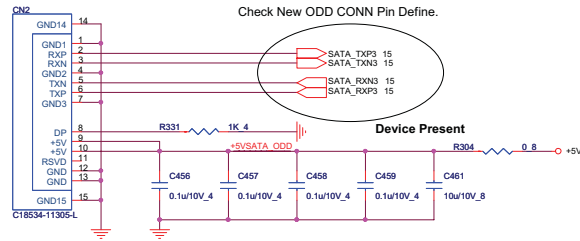
4/10 remove Flash card ckt



SATA ODD

9/28 change to SATA ODD conn to BD3G use

10/22 update footprint to SATA-C18534-11305-13P-R

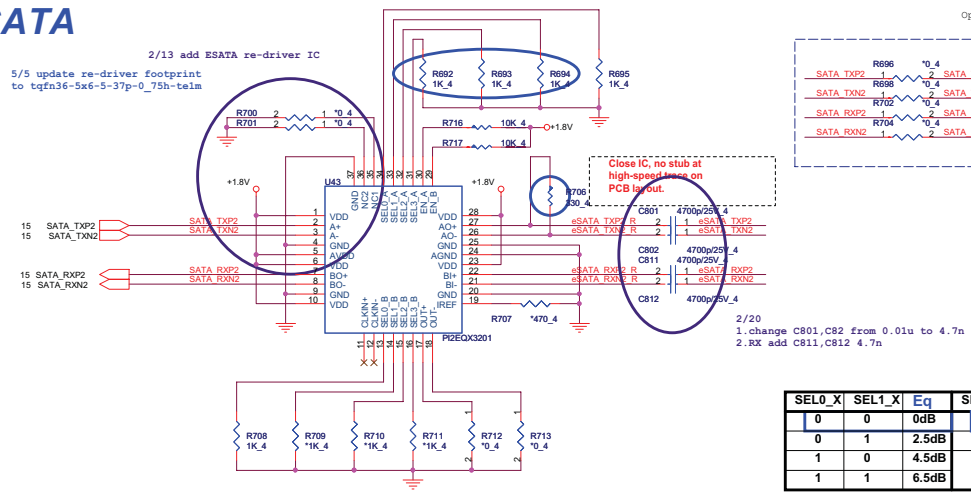


4/14 change R706 from 0 ohm to 330 , stuff R692,R693,R694

ESATA

2/13 add ESATA re-driver IC

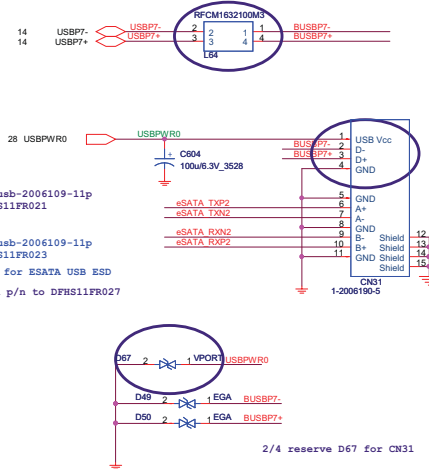
5/5 update re-driver footprint to tqgn36-5x6-5-37p-0_75h-teim



SEL0_X	SEL1_X	Eq	SEL2_X	Swing	SEL3_X	De-Emphasis
0	0	0dB	0	1.0X	0	0dB
0	1	2.5dB	1	1.2X	1	-3.5dB
1	0	4.5dB				
1	1	6.5dB				

Co-lay ESATA footprint

2/29 del R572,R569

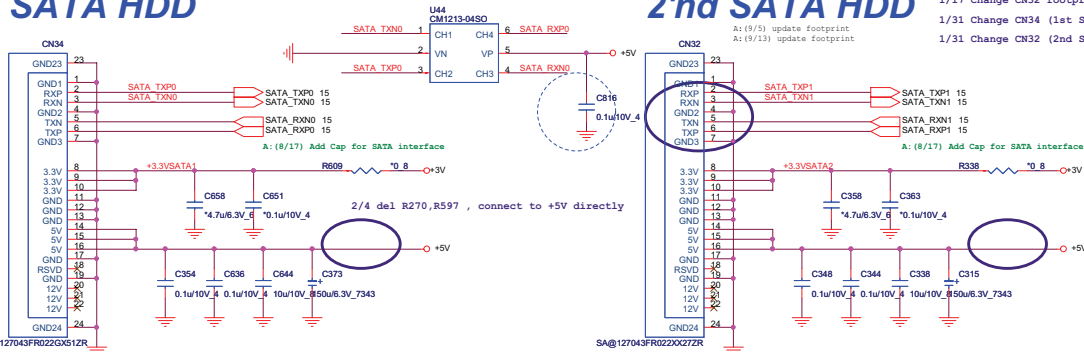


4/17 remove D77-D81 for CN34 , change to U44 CM1213-04SO

5/5 add C816 0.01u to U44 +5V for ESD

SATA HDD

2'nd SATA HDD



1/17 Change CN32 (2nd SATA CONN) from DFHS22FR064 to DFHS22FR094

1/17 Change CN32 footprint from SATA-127043FR022XX272R-22P-L-H to SATA-127043FR022G2852R-22P-L

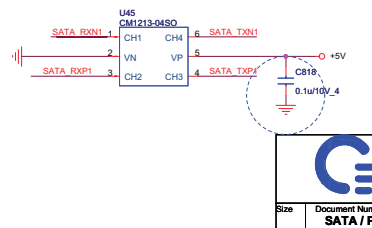
1/31 Change CN34 (1st SATA) P/N from DFHS22FR063 to DFHS22FR082

1/31 Change CN32 (2nd SATA) P/N from DFHS22FR094 to DFHS22FR083

2/4 reserve D82-D86 for CN32 (2ND HDD)

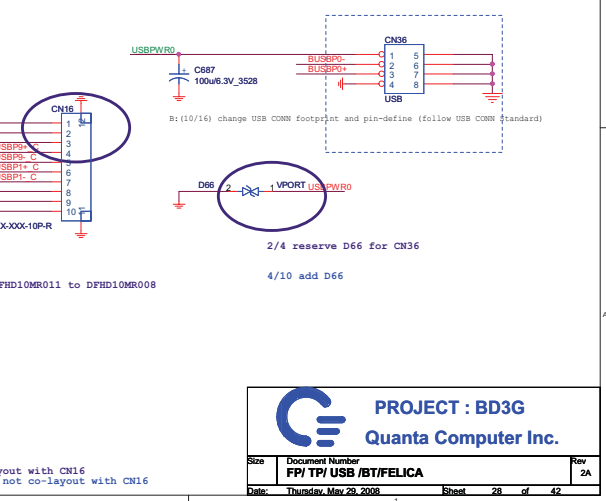
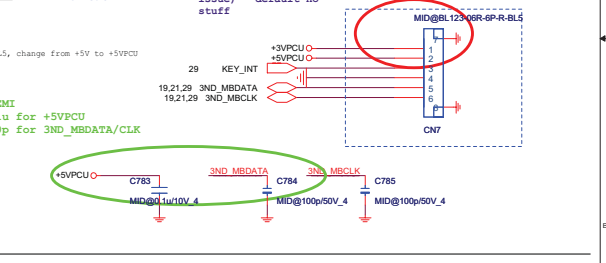
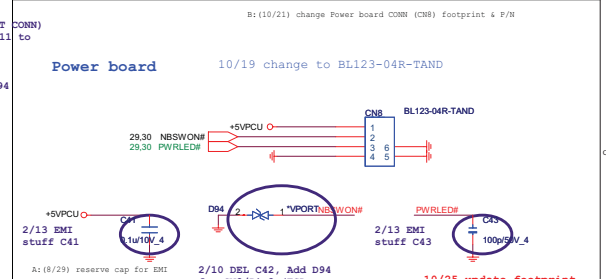
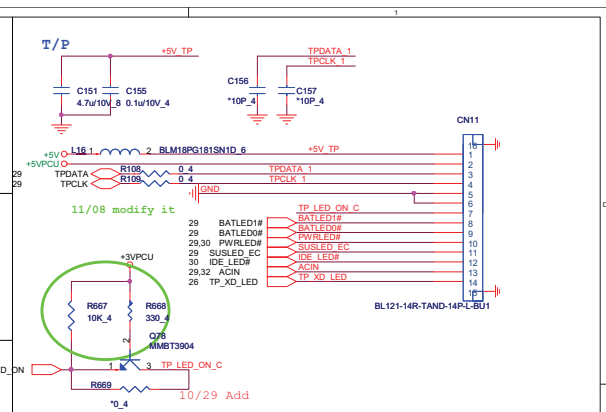
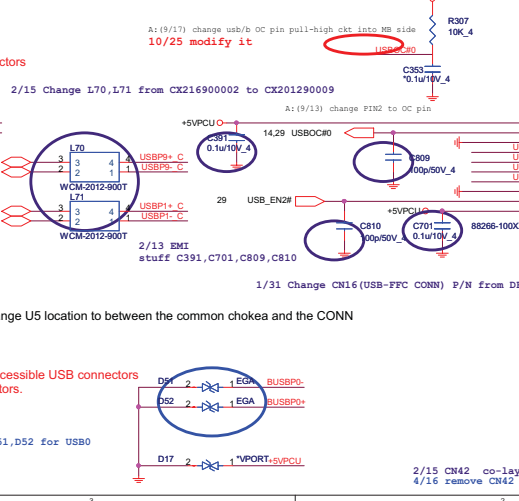
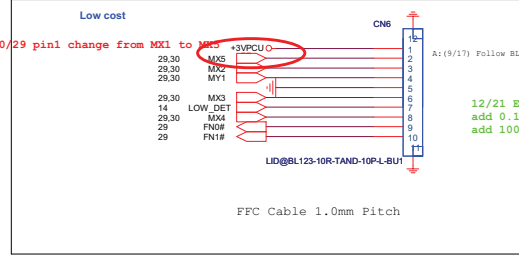
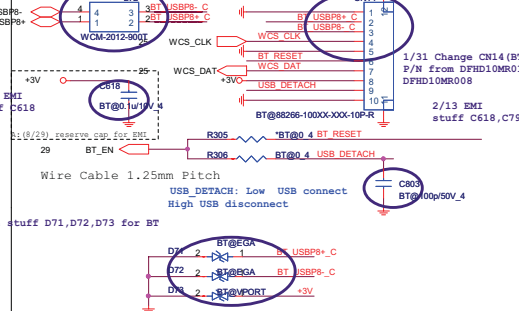
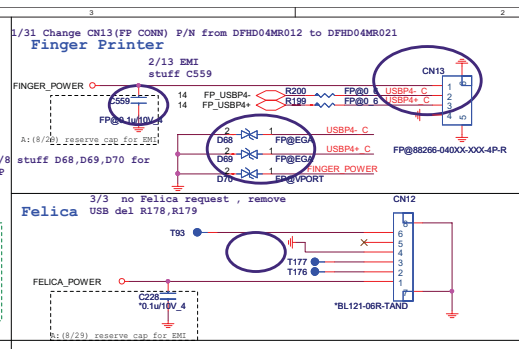
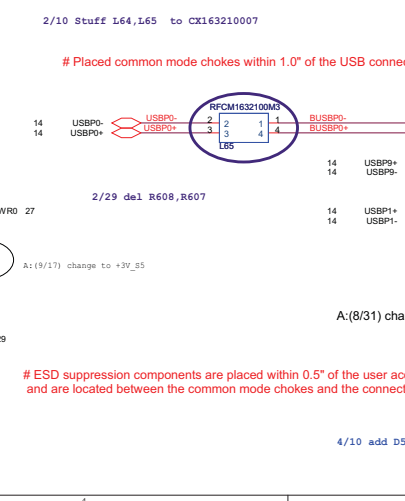
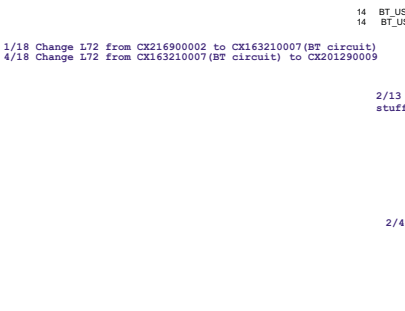
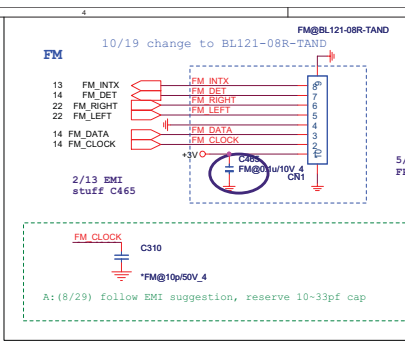
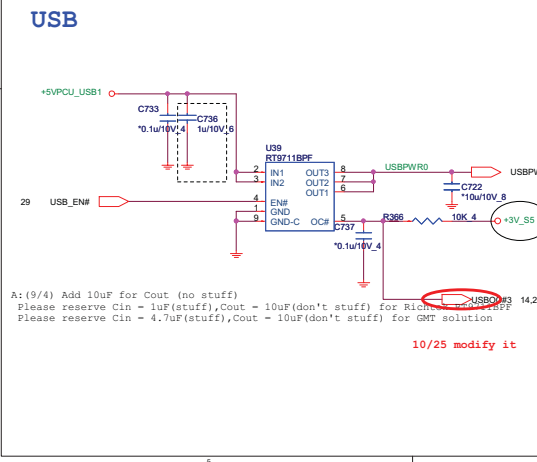
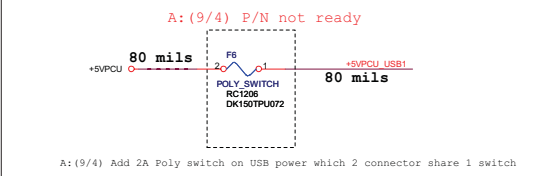
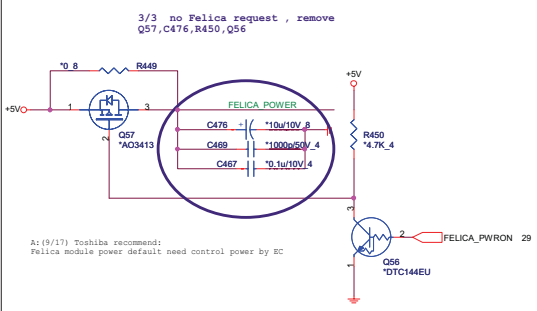
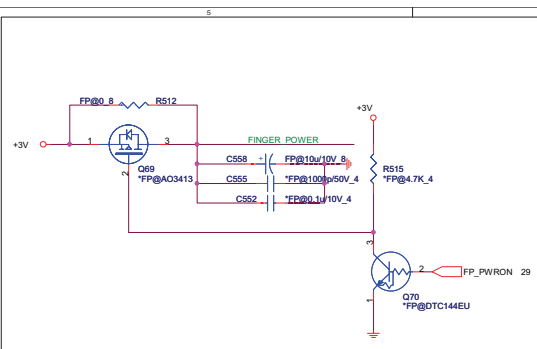
4/17 remove D82-D86 for CN32 , change to U45 CM1213-04SO

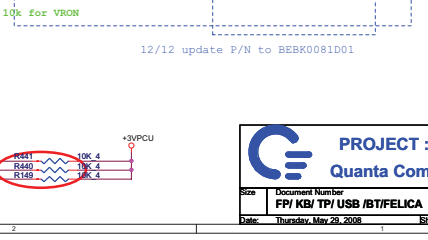
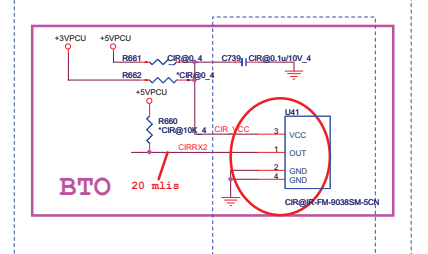
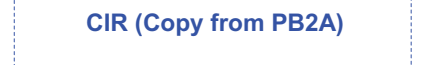
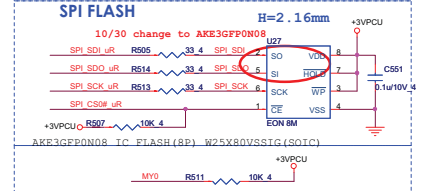
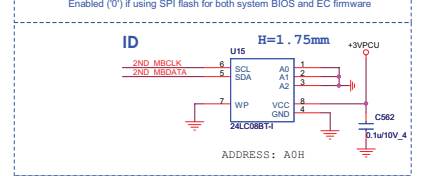
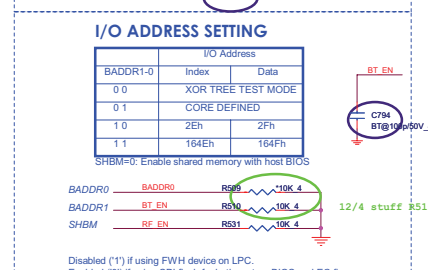
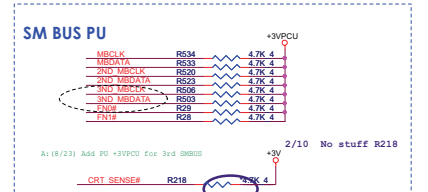
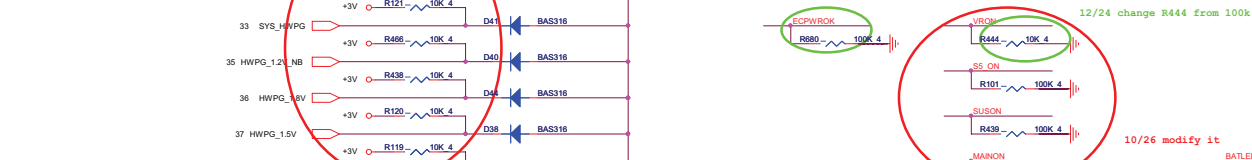
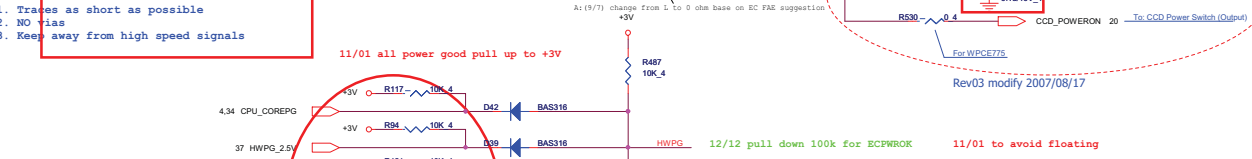
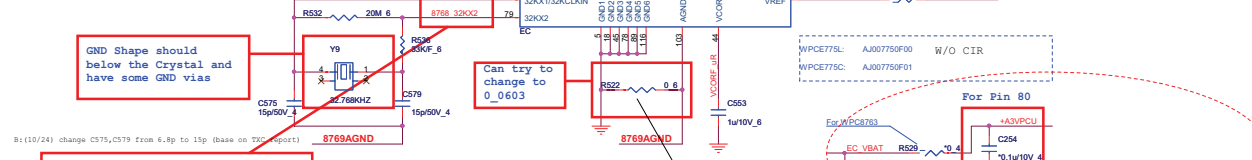
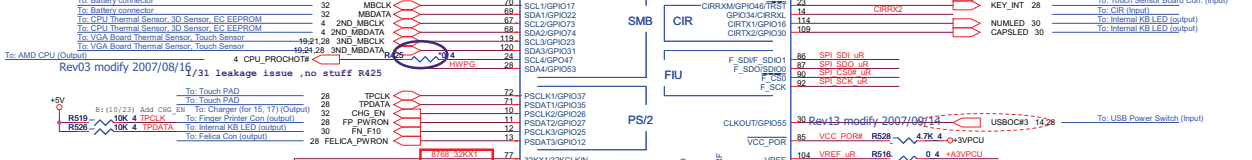
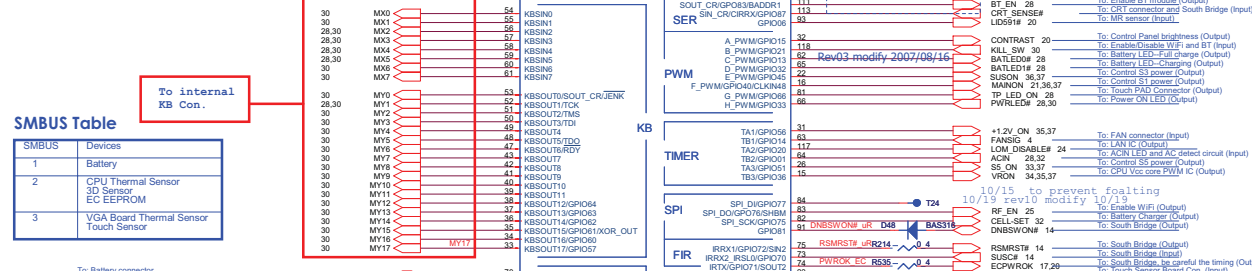
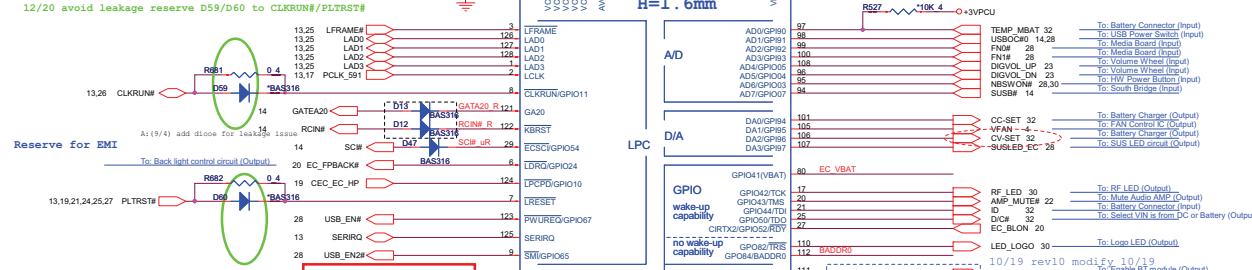
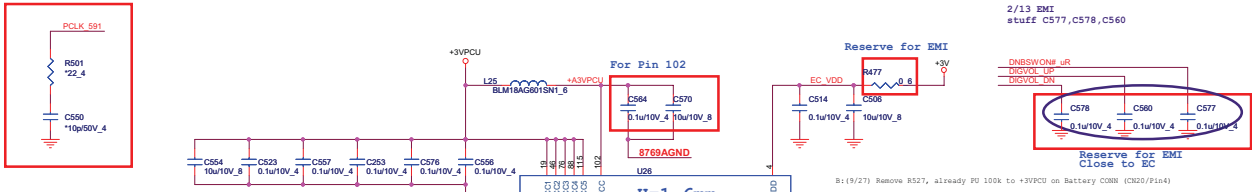
5/5 add C818 0.01u to U45 +5V for ESD



PROJECT : BD3G
Quanta Computer Inc.

Size	Document Number	Rev
	SATA / PATA	2A
Date:	Thursday, May 29, 2008	Sheet 27 of 42





1. Traces as short as possible
2. NO vias
3. Keep away from high speed signals

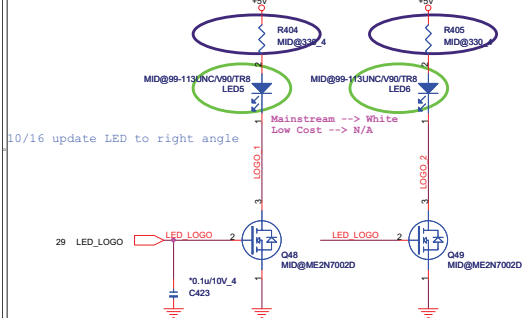
SMBUS	Devices
1	Battery
2	CPU Thermal Sensor 3D Sensor EC EEPROM
3	VGA Board Thermal Sensor Touch Sensor

PROJECT : BD3G
Quanta Computer Inc.

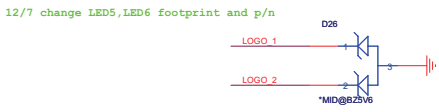
Size	Document Number	Rev
	FP/ KB/ TP/ USB /BT/FELICA	2A
Date:	Thursday, May 29, 2008	Sheet 29 of 42

2/1 Change R404,R405 from CS13902JB14 (390 ohm) to CS13302JB21(330 ohm)

LOGO LED

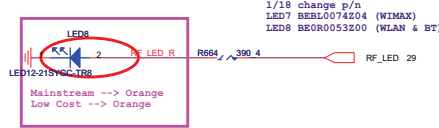


10/16 update LED to right angle



12/7 change LED5,LED6 footprint and p/n

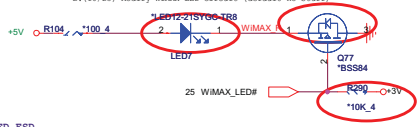
W-LAN&BT



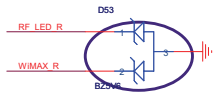
1/18 LED7,8 change footprint from LED12-21SYGC-TR8 to LED27-21-BHC-Z11M27Y-3C

1/18 change p/n
LED7 BEBL0074204 (WIMAX)
LED8 BEOR0053200 (WLAN & BT)

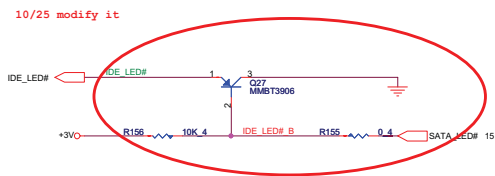
WiMAX LED



5/8 stuff D53 for RF_LED_ESD

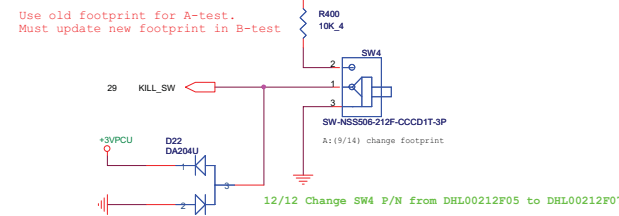


IDE LED



10/25 modify it

Kill SW



Use old footprint for A-test.
Must update new footprint in B-test

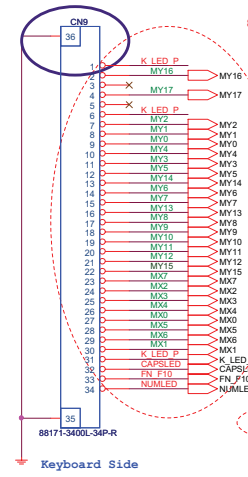
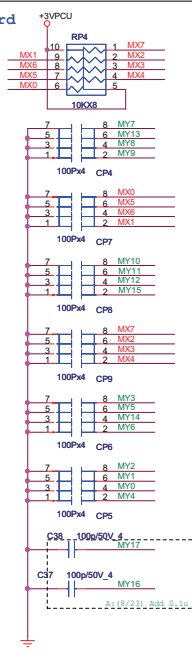
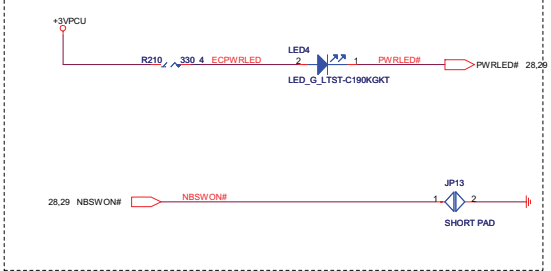
1/18 Change SW4 footprint from SW-NSS506-212F-CCCD1T-3P to SW-NSS506-212F-CCCD1T-3P-BD3A (SMT open issue)

12/12 Change SW4 P/N from DHL00212F05 to DHL00212F07

Keyboard

1/18 change footprint from 88171-3400L-34P-L to 91504-340N-34P-L

Jumper & LED (debug use)



8/15 Modify Keyboard pin define

2/13 EMI stuff C39,C436

1/17 Remove CN10 (Keyboard CONN)

8/15 Add K_LED_P power

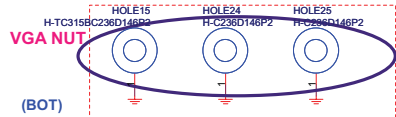
A:(8/27) Confirm with EC FAE,
MY no need External PU resistor

	15"	17"
CAPSLED	V	V
K_LED_P (Pin 31)	V	V
FN_F10 K_LED_P (Pin 6)	V	V
NUMLED K_LED_P (Pin 1)	V	V

HOLE

Take care NUT P/N base on IV/EV sku

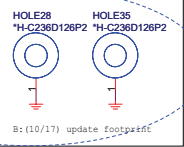
1/18 HOLE 17,18,23 FBBL5004010 change to FBBL5002010



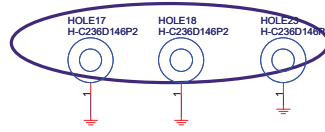
MDC NUT (BOT)



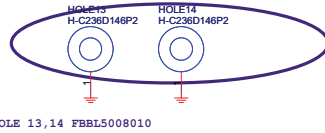
Mini-PCI-A NUT (BOT)



CPU NUT (BOT)



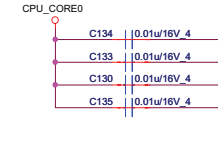
Mini-PCI-B NUT (BOT)



NUT P/N Control Table

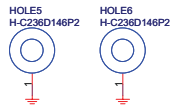
	UMA sku	EV sku
HOLE15	FBBL5002010	FBBD3021010
HOLE24	FBBL5002010	FBBD3021010
HOLE25	FBBL5002010	FBBD3021010

Stitch CAP



10/31 EMI request
2/18 HOLE 15,24,25 FBBD3017010 change to FBBD3021010

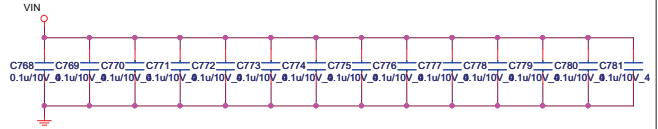
KB NUT (TOP)



2/18 HOLE 28,35 FBBL5007010 change to FBBL5050010
5/5 remove HOLE28,35 (HD Decoder)

2/18 HOLE 13,14 FBBL5008010 change to FBBL5051010
4/17 update HOLE13,14 footprint to H-C236D146P2

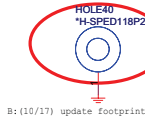
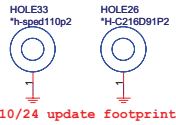
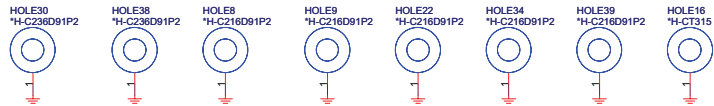
For fix HyperTransport nets across plane splits



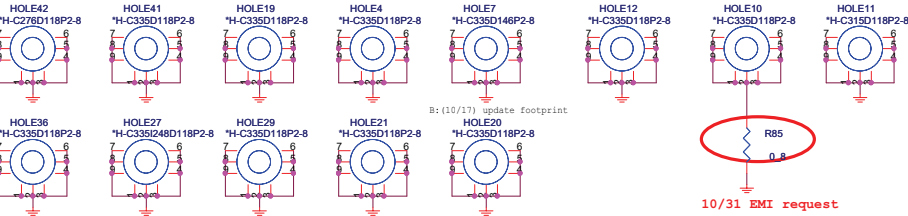
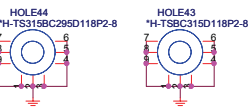
E-SATA NUT (BOT)



4/21 remove Hole31,37



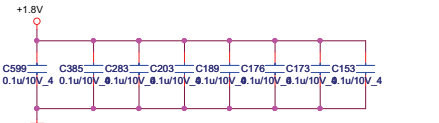
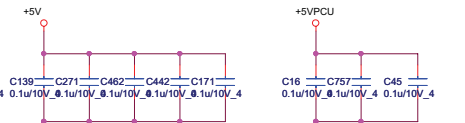
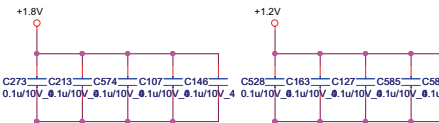
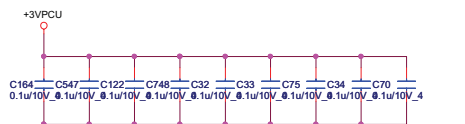
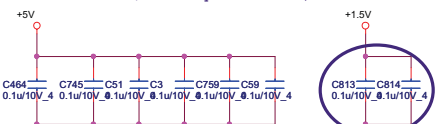
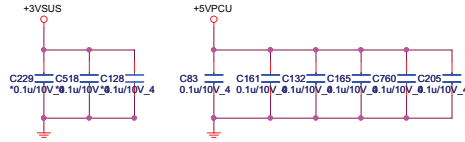
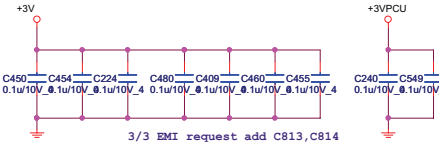
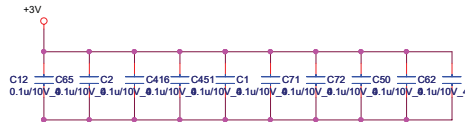
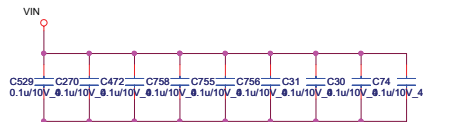
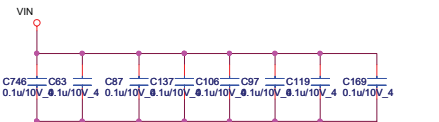
10/24 update footprint



10/31 EMI request

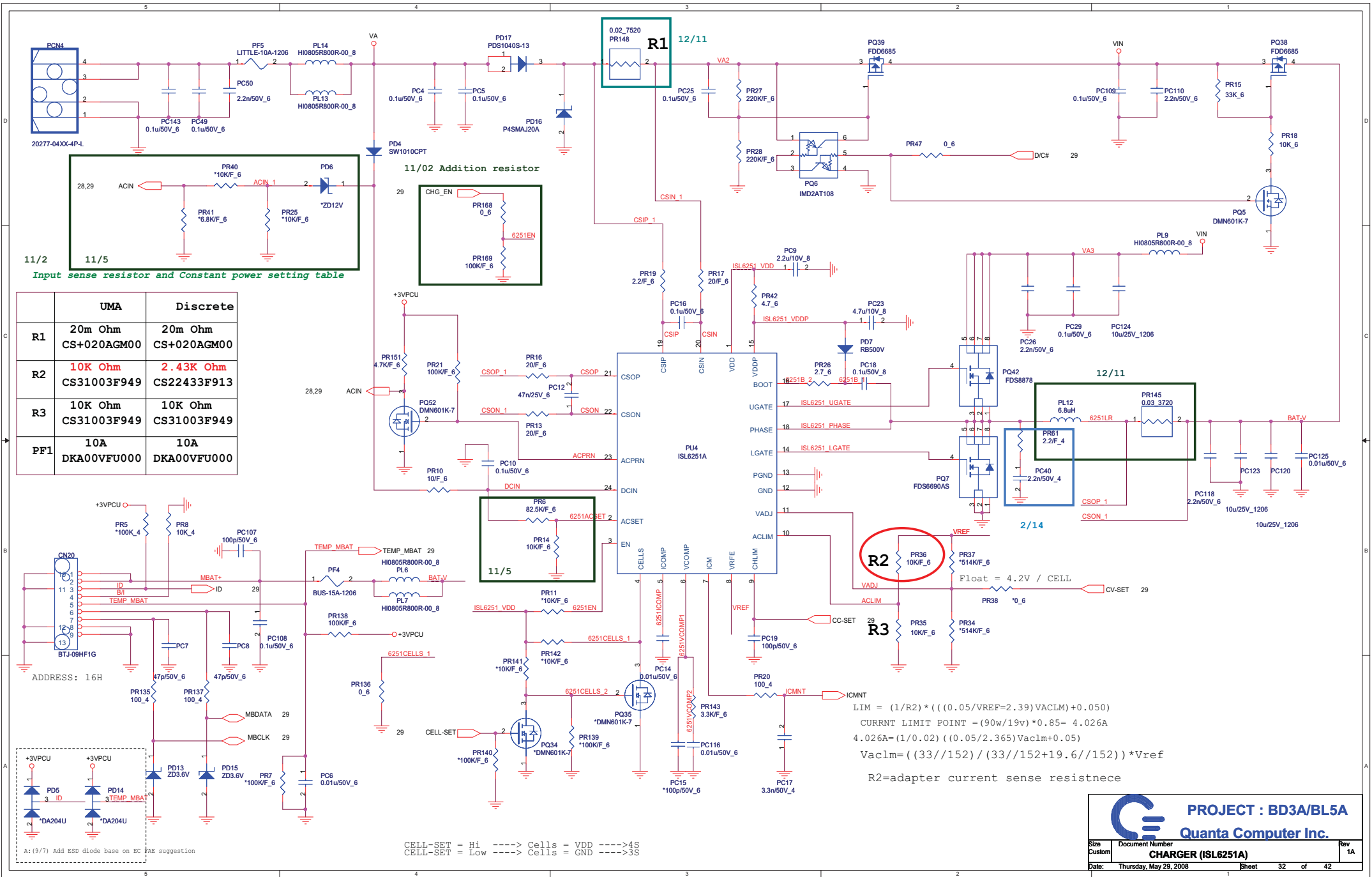
RAMP:(1/16) Follow BL5, update Hole footprint (13pcs)

EMI CAP.



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Quanta Computer Inc.

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	HOLE/EMI CAP/ESD PAD	2A
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11/2
11/5
Input sense resistor and Constant power setting table

	UMA	Discrete
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	10K Ohm CS31003F949	2.43K Ohm CS22433F913
R3	10K Ohm CS31003F949	10K Ohm CS31003F949
PF1	10A DKA00VFU000	10A DKA00VFU000

11/5	PR3 82.5K/F_6	6251ACSET 2
	PR14 10K/F_6	

2/14	PR26 10K/F_6	PR37 *514K/F_6
	PR35 10K/F_6	PR34 *514K/F_6

CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S

$$LIM = (1/R2) * (((0.05/VREF=2.39) VACLm) + 0.050)$$

$$CURRNT LIMIT POINT = (90w/19v) * 0.85 = 4.026A$$

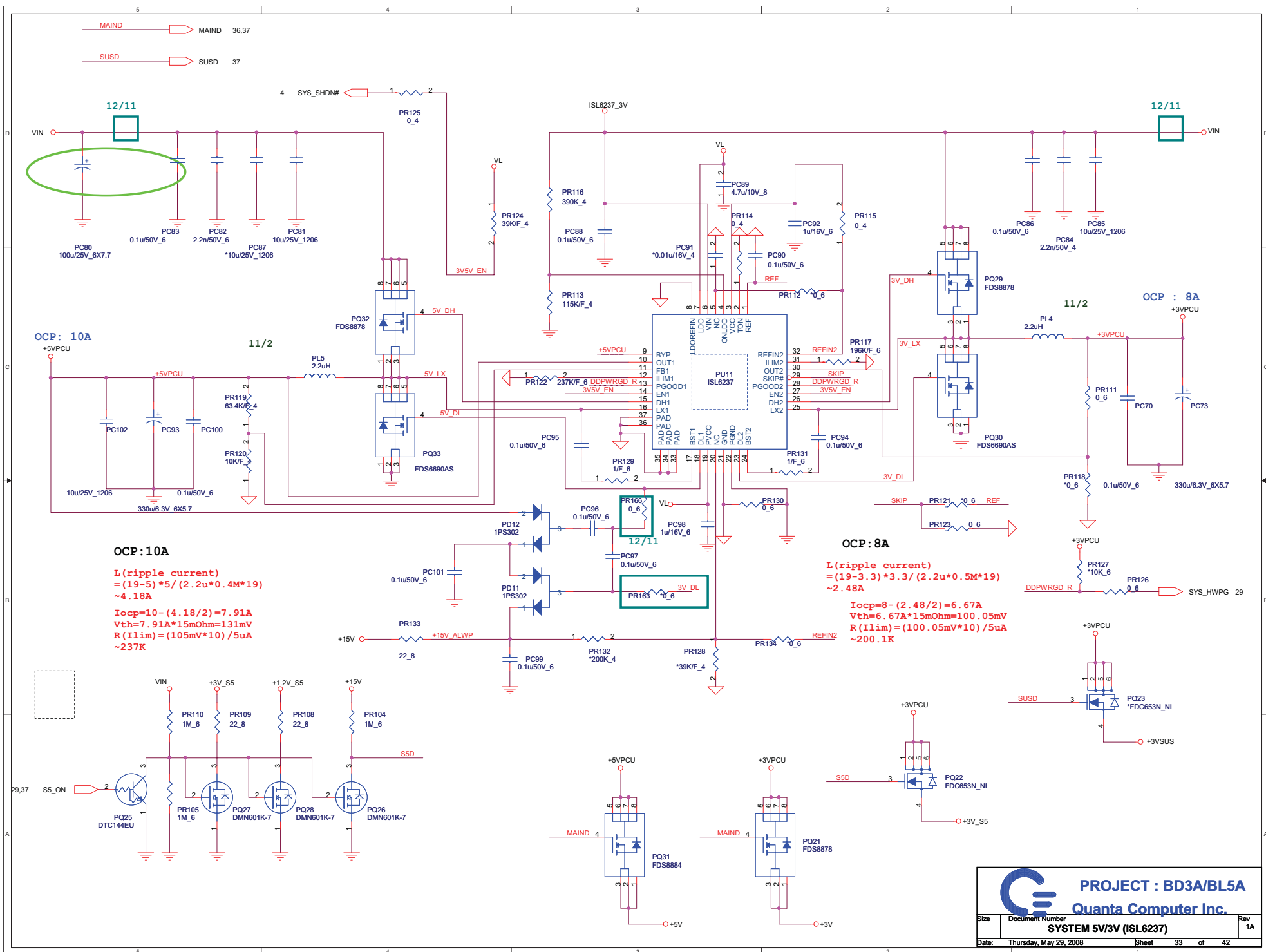
$$4.026A = (1/0.02) * (((0.05/2.365) VACLm) + 0.05)$$

$$VACLm = ((33//152) / (33//152 + 19.6//152)) * Vref$$

R2=adapter current sense resistnece

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OCP: 10A

OCP: 10A

$L(\text{ripple current})$
 $= (19-5) * 5 / (2.2u * 0.4M * 19)$
 $\sim 4.18A$
 $I_{ocp} = 10 - (4.18/2) = 7.91A$
 $V_{th} = 7.91A * 15m\Omega = 131mV$
 $R(I_{lim}) = (105mV * 10) / 5uA$
 $\sim 237K$

OCP: 8A

$L(\text{ripple current})$
 $= (19-3.3) * 3.3 / (2.2u * 0.5M * 19)$
 $\sim 2.48A$
 $I_{ocp} = 8 - (2.48/2) = 6.67A$
 $V_{th} = 6.67A * 15m\Omega = 100.05mV$
 $R(I_{lim}) = (100.05mV * 10) / 5uA$
 $\sim 200.1K$


PROJECT : BD3A/BL5A
Quanta Computer Inc.
SYSTEM 5V/3V (ISL6237)

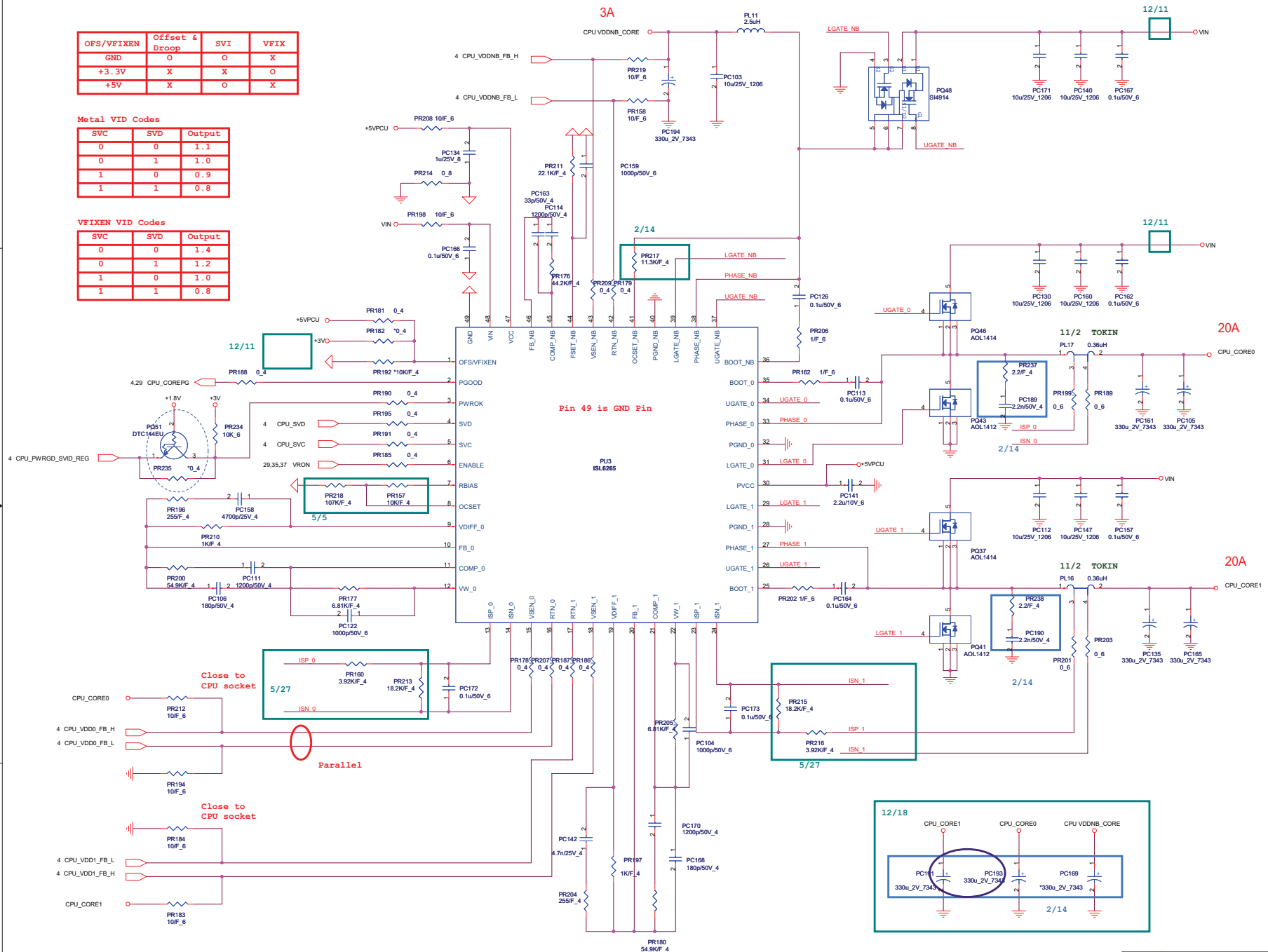
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		1A

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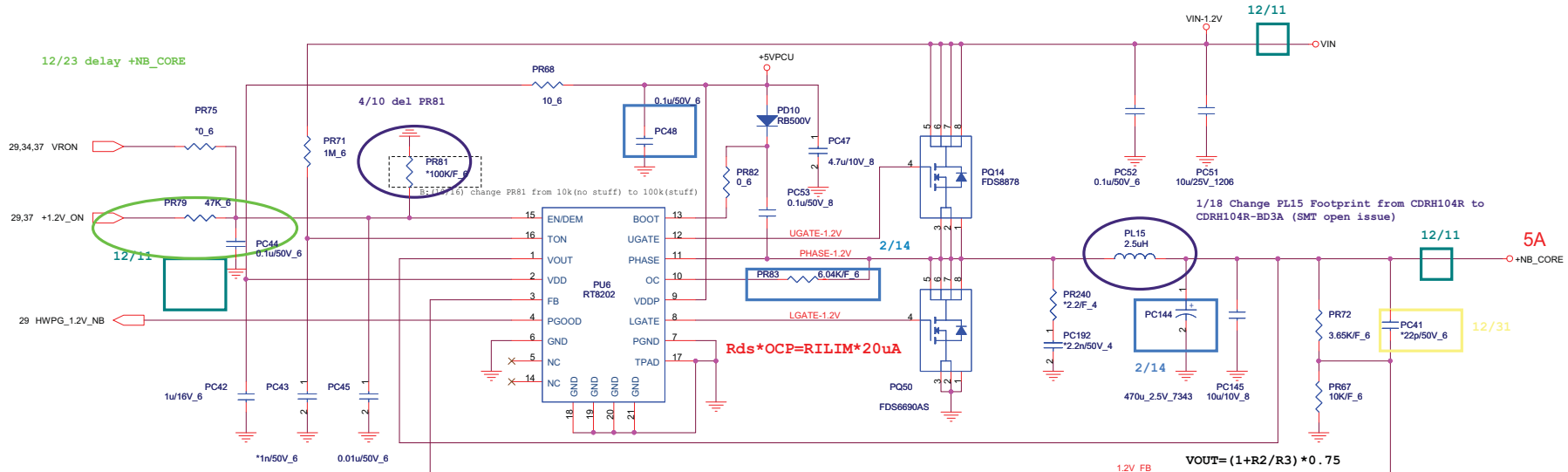
OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	0	0	X
+3.3V	X	X	0
+5V	X	0	X

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



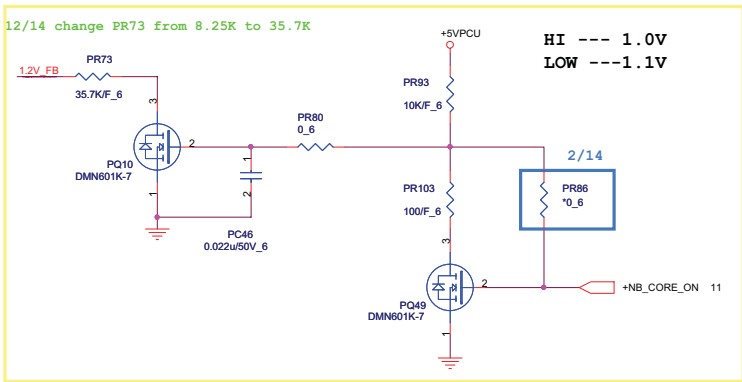
4/10 add PC191,PC193



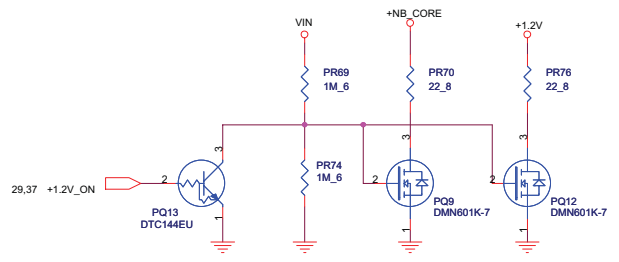
$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$

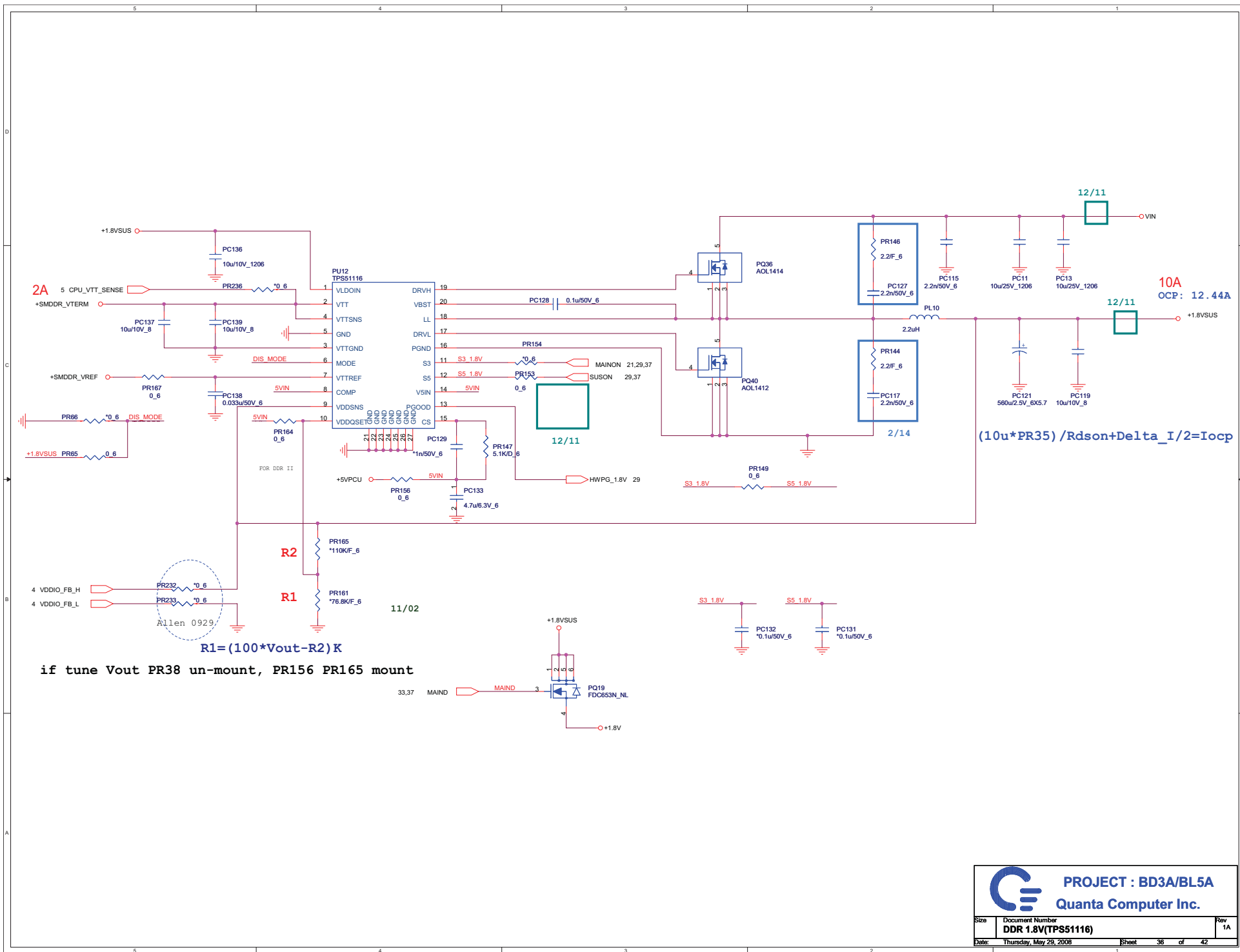
6A OCP --- $OC = 4.53K$
FDS6690AS $R_{ds} = 15m\Omega$

$R_{ds} * OCP = R_{ILIM} * 20uA$



12/14 del +1.35V_VDDHTTX
 PU15
 PC180, PC182, PC179
 PR227, PR226, PR225





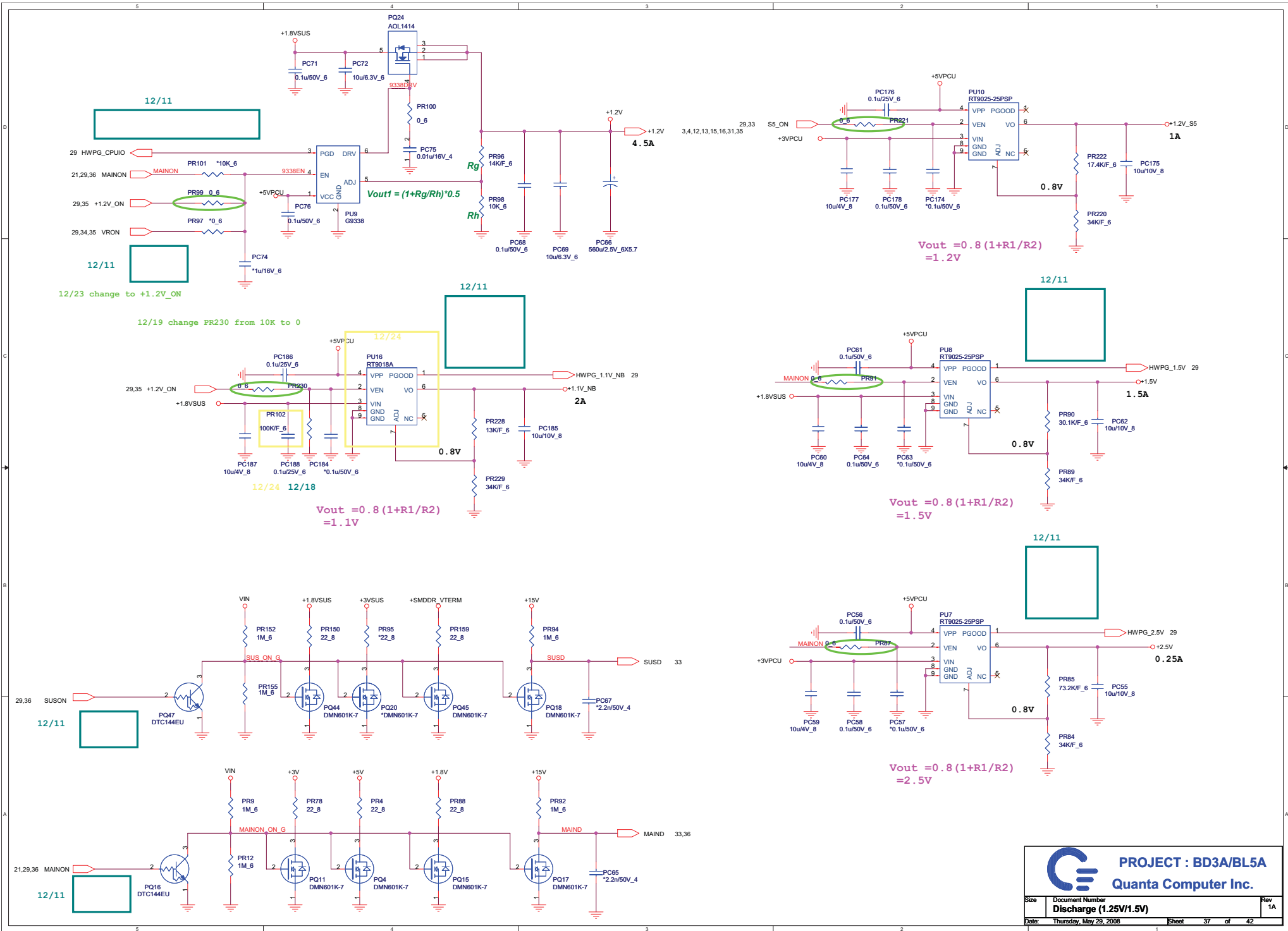
2A

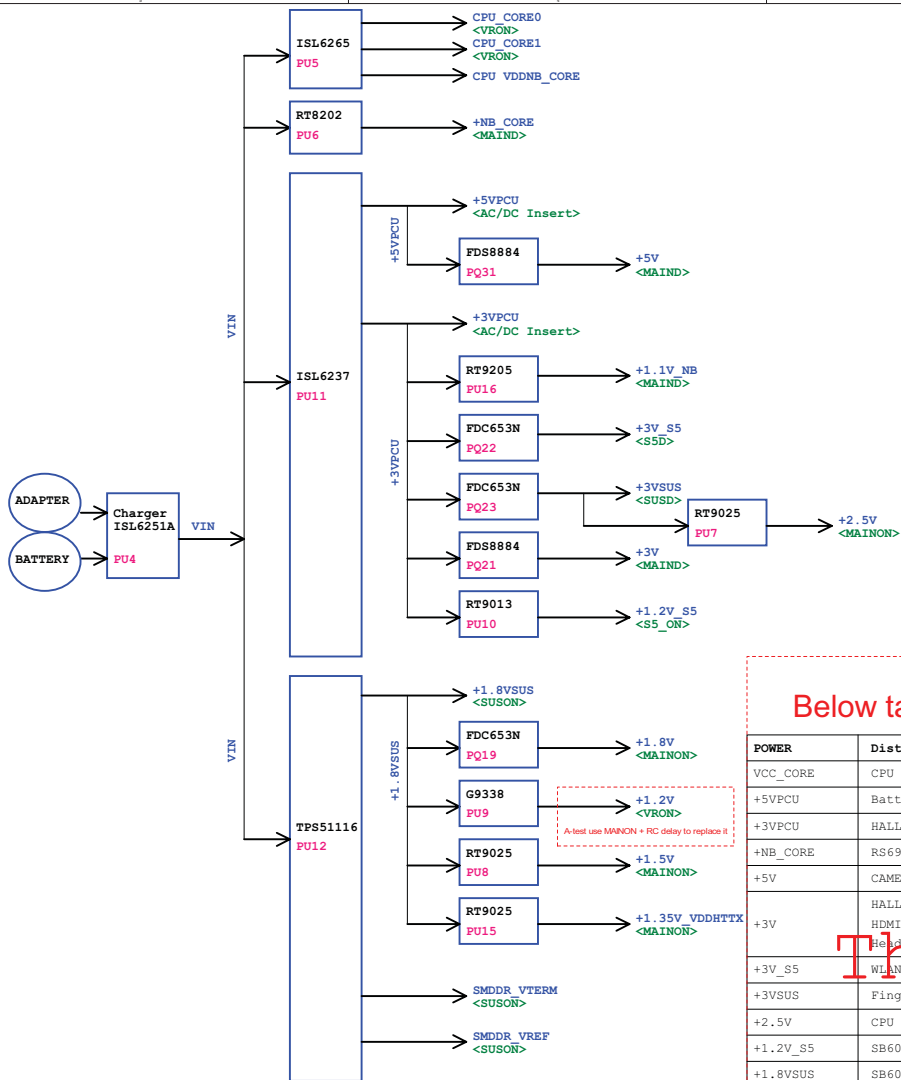
10A
OCP: 12.44A

$$(10u \cdot PR35) / R_{dson} + \Delta I / 2 = I_{ocp}$$

$$R1 = (100 \cdot V_{out} - R2) K$$

if tune Vout PR38 un-mount, PR156 PR165 mount

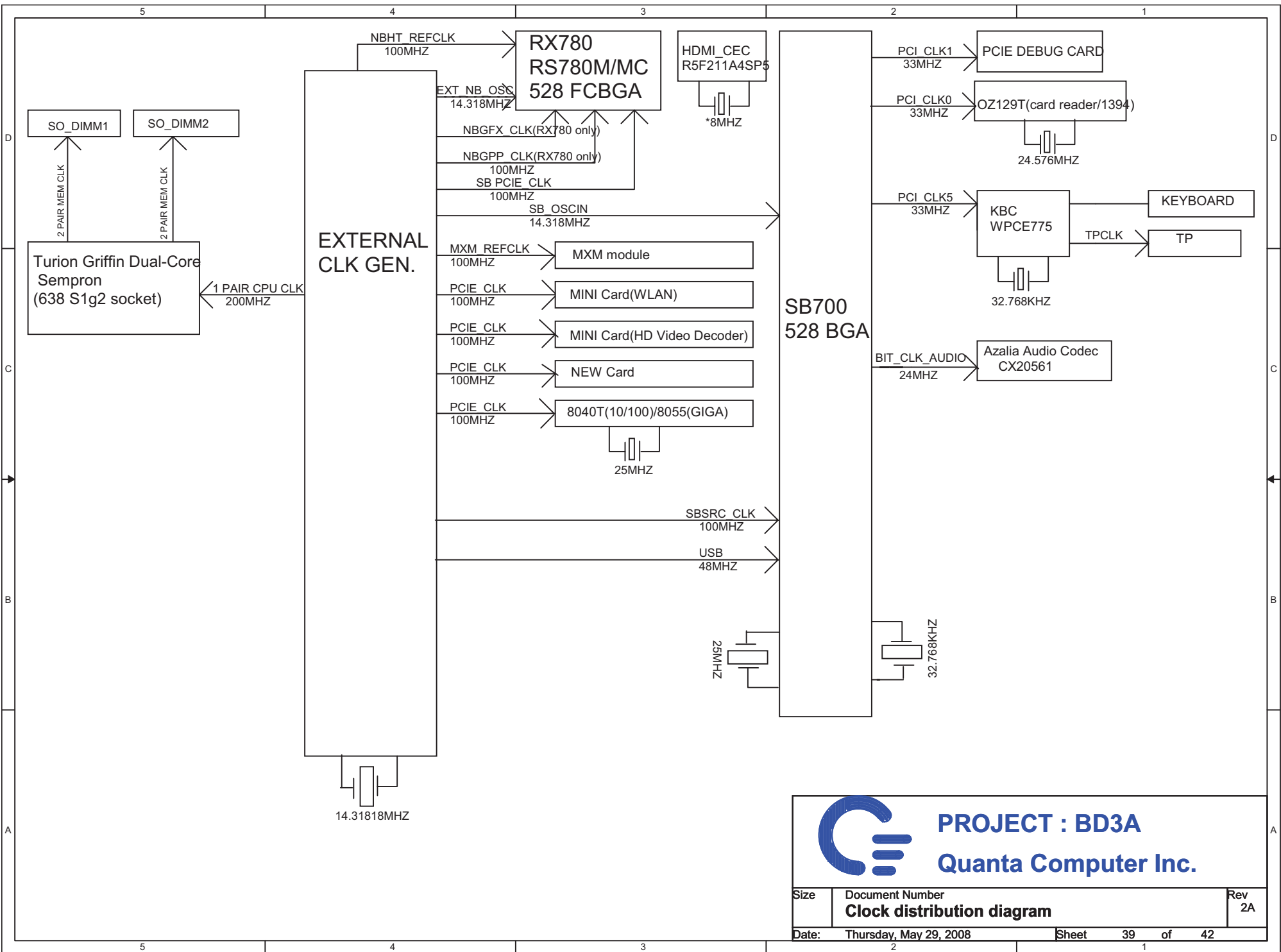




Below table need be modify (waiting other schematic ready)

POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_CORE	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Modem (CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	


The Table NOT READY



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Quanta Computer Inc.

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	Clock distribution diagram	2A
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Model	REV	DATE	CHANGE LIST	NOTE	
BD3G	A1A	2007	FIRST RELEASED : Import BOM ECN	ECN Release	
		20071008	PAGE23:Reverse U42,C761 for VR	Circuit modify	
		20071008	PAGE28:Add R667,R668,Q78 for TP_LED	Circuit modify	
		20071204	PAGE04:Reverse C762 for AMD engineer CPU use	Circuit modify	
		20071204	PAGE19:update CN25 HDMI footprint to HDMI-C12816-119A5-L-19P-V-BL5-1	Circuit modify	
		20071204	PAGE15:change BOARD ID3 from GEVENT7 to GPIO48	Circuit modify	
		20071204	PAGE14:change BOARD ID PD value from 10K to 1K(R227,R228,R229,R248,R343,R236)	Circuit modify	
		20071204	PAGE29:Stuff R510, no-stuff R509 (slope BT module can't bring up issue)	Circuit modify	
		20071204	PAGE20: modify display on ckt to avoid flash when into S3/S4/S5 (add Q78,Q80,R670,del Q41,R388)	Circuit modify	
	B2A	20071207	PAGE19:update CN25 HDMI footprint to HDMI-C12816-119A5-L-19P-H-BD3	Circuit modify	
		20071207	PAGE32:update ACIN design	Circuit modify	
		20071207	PAGE24:Change R449(0 ohm) to D56(Diode) for leakage issue (3VPCU to 3V_S5)	Circuit modify	
		20071207	PAGE23: Slove Audio issue:When plug in-out headphone, headphone has no sound. 1. Change R652&R651 to C763,C764(10U/6.3V 0603)	Circuit modify Circuit modify	
		20071207	PAGE22: Remove D19 to slove Audio issue Switch Mute to Un-mute, sound will delay about 2 seconds.	Circuit modify	
		20071207	PAGE14: add D57,D58 to avoid voltage leakage	Circuit modify	
		20071207	PAGE30:update LED5,LED6 footprint and PN	Circuit modify	
		20071207	PAGE04:add R671~R679 for AMD request	Circuit modify	
		20071208	PAGE03:change C223 C225 from 10p to 33p PAGE15:change C257 C258 from 10p to 27p PAGE26:change C380 C381 from 22p to 18p		
		20071210	PAGE25:Change New card footprint to NCARD-13180151-T-26P-L-BL55		
		20071210	PAGE22:stuff R372 for FM		
		20071211	update power		
		20071212	PAGE29: Change U41(CIR) from BEBK0081D00 to BEBK0081D01		
		20071212	PAGE18: Change CN22(S-Video) from DFMD04FR296(Yellow Color) to DFMD04FR006(Black Color)		
		20071212	PAGE30: Change SW4 P/N from DHL00212F05 to DHL00212F07		
		20071212	PAGE31: Update Hole43 H-TSBC315D118P2, Hole 44 H-TS315BC295D118P2		
		20071212	PAGE29: pull down 100k R680 for ECPWROK		
		20071212	A11 to A12 implemen		
			PAGE12: Del L15 stuff L36		
			PAGE16: Del R234 stuff R235		
			PAGE35: Del PU15,PC180,PC182,PC179PR227,PR226,PR225, Change PR73 from 8.25K to 35.7K		
		20071220	PAGE23: Slove GPRS noise 1. stuff R386/R387/C404/C405 to 0.1u 2. Change L44/41 to BK1608LL121		
		20071220	PAGE29: avoid leakage reserve D59/D60 to CLKRUN#/PLTRST#		
		20071221	PAGE18:add 27p(C790~C793) for TV_Y/G , TV_C/R		
		EMI	PAGE21:stuff C568,C548		
			PAGE22:stuff R399,R379		
			PAGE23:Change L43/44 to BK1608LL121		
			PAGE24:add L74,C766,C767,C789,C788 for +2.5V_1.8V_LAN,add L73 for +1.2V_LAN		
			PAGE26:add 0 ohm and 22p for SD/MS CLK , R308~R329 0ohm(CS00002JB38) change to 33ohm(CS03302JB29), remove RN34,RN35, stuff L68,L69 for 1394		
			PAGE28:del R276,R278 stuff L72 , del R613,R612,R624,R626 stuff L70,L71 , add 0.1u for +5VPCU add 100p for 3ND_MBDATA/CLK		
			PAGE31:stuff all 0.1 cap		
		20071221	update power		
		20071222	PAGE11: stuff R48 2.2K for power play		
		20071222	PAGE24: Per cost down remove LAN eeprom,stuff R381,remove U21,R380,R378		
		C3A	20080102	PAGE14: NEW_DET# change from Geven3# to GPM1#	
			20080117	Update RX781	
		20080117	PAGE13:Modify RTC circuit. R301,R302 change from 8.66k to 2k. R332 change from 4.7K to 6.8K		
		20080117	PAGE13:Change RTC Battery from VARTA (AHL03001441) to MATSUSHITA (AHL03002005)		
		20080117	PAGE19:Change back HDMI connector(CN25) footprint from HDMI-C12816-119A5-L-19P-H-BD3 to HDMI-C12816-119A5-L-19P-H-BL5(SMT open issue)		
		20080117	PAGE20:for engery star add R684 connect to EC pin27		
		20080117	PAGE24:Change CN28 (RJ45 CONN) from DFTJ12FR024 to DFTJ12FR035		
		20080117	PAGE27:Change CN32(2nd SATA CONN) from DFHS22FR064 to DFHS22FR094		
		20080117	PAGE27:Change CN32 footprint from SATA-127043FR022XX27ZR-22P-L-H to SATA-127043FR022G285ZR-22P-L		
		20080117	PAGE30:Remove CN10 (Keyboard CONN)		
		20080117	PAGE21:Remove R492,R517, Short CN27/Pin189,190 to VIN directly.		
		20080118	PAGE28:Change L72 from CX216900002 to CX163210007(BT circuit)		
		20080118	PAGE08:Change CN19 footprint from DDR-C-292564-200P to DDR-C-292564-200P-BD3A (SMT open issue)		
		20080118	PAGE08:Change CN23 footprint from DDR-C-1734071-200P to DDR-C-1734071-200P-BD3A (SMT open issue)		
		20080118	PAGE30:Change SW4 footprint from SW-NSS506-212F-CCCD1T-3P to SW-NSS506-212F-CCCD1T-3P-BD3A (SMT open issue)		
		20080118	PAGE23:Change CN43 footprint from MDC-1-179373-2-12P-RUV to MDC-1-179373-2-12P-RUV-BD3A (SMT open issue)		
		20080118	PAGE35:Change PL15 Footprint from CDRH104R to CDRH104R-BD3A (SMT open issue)		
		20080118	PAGE22:Add R685 for VISTA WHQL circuit		
		20080118	PAGE24: Change RJ45 footprint from LAN-100073FR012G101ZL-12P to rj45-c100s7-10806-I-12P		
		20080118	PAGE31:HOLE 17,18,23 FBBL5004010 change to FBBL5002010		



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Model	REV	DATE	CHANGE LIST	NOTE
BD3G	C3A	20080118	PAGE30:change footprint from 88171-3400L-34P-L to 91504-340N-34P-L	Circuit modify
		20080118	PAGE30:LED7,8 change footprint from LED12-21SYGC-TR8 to LED27-21-BHC-ZL1M2TY-3C	Circuit modify
		20080118	PAGE30:change p/n LED7 BEBL0074Z04 (WIMAX),LED8 BE0R0053Z00 (WLAN & BT)	Circuit modify
		20080131	PAGE31:update HOLE42,41,19,4,7,12,10,11,36,27,29,21,20,43,44	Circuit modify
		20080131	voltage leakage issue	Circuit modify
		20080131	PAGE04:modify CPU_PROCHOT# ckt (add R687, no stuff R686,R425), CPU_LDT_REQ#, CPU_PWRGD connect to +1.8V	Circuit modify
		20080131	PAGE11:remove Q5,Q3,R83,R80,R97,stuff R88,R77	Circuit modify
		20080131	PAGE14:BOARD_ID4 change from GPIO66 to GPIO3	Circuit modify
		20080131	PAGE14:NEW CARD hot plug issue_NEW_DET# change from GEVEN5# to GPM1# (SB700 A12 Errata)	Circuit modify
		20080131	PAGE19: DEL L56,L57,L58,L59,R465,R474,R493,R495,R486,R488,R478,R483,C226,C227 for HDMI circuit	Circuit modify
		20080131	PAGE25: add +3V to CN21 pin39,41	Circuit modify
		20080131	PAGE18: Change L4,L5,L6 to CX8BA470003 to meet CRT spec	Circuit modify
		20080131	PAGE19: Change U11 from ARBL5SV0000 to ARBL5MV0000	Circuit modify
		20080131	PAGE28:According to customer request, we can't stuff C782 (22pF) in SD/MS_CLK	Circuit modify
		20080131	PAGE25: Change R573 from 28.7K to 0 ohm, Remove C628 for NEW card some device can't work normal	Circuit modify
		20080131	PAGE14: Change R350 from 1K to 0 ohm (Slove VCCRTC can't reach 0V when clear CMOS.)	Circuit modify
		20080131	PAGE28: Change CN33(5 in 1 card CONN) P/N from DFHS38FR003 to DFHS38FR005	Circuit modify
		20080131	PAGE27: Change CN34 (1st SATA) P/N from DFHS22FR063 to DFHS22FR082	Circuit modify
		20080131	PAGE27: Change CN32 (2nd SATA) P/N from DFHS22FR094 to DFHS22FR083	Circuit modify
		20080131	PAGE20: Change CN5 (I-MIC)P/N from DFHD02MR003 to DFHD02MR016	Circuit modify
		20080131	PAGE22: Change CN39(I-MIC CONN) P/N from DFHD02MR003 to DFHD02MR016	Circuit modify
		20080131	PAGE22: Change CN17(SPK CONN) P/N from DFHD04MR012 to DFHD04MR021	Circuit modify
		20080131	PAGE28: Change CN16(USB-FFC CONN) P/N from DFHD10MR011 to DFHD10MR008	Circuit modify
		20080131	PAGE28: Change CN13(FP CONN) P/N from DFHD04MR012 to DFHD04MR021	Circuit modify
		20080131	PAGE28: Change CN14(BT CONN) P/N from DFHD10MR011 to DFHD10MR008	Circuit modify
		20080201	PAGE22: Change INT-SPK AMP GAIN VALUE. Change R623,R625 from 9.1k to 5.1k 1%,Change R620,R621 from 10k to 16k 1%	Circuit modify
		20080201	PAGE30: Change R404,R405 from CS13902JB14 (390 ohm) to CS13302JB21(330 ohm)	Circuit modify
		20080201	RS780M A13 Errata	Circuit modify
		20080201	PAGE11:change R103 from 150 to 140 CS11402FB01	Circuit modify
		20080201	PAGE18:RS780M A13 R8 ----> 140 CS11402FB19,MXM R8 ----> 150 CS11502FB21	Circuit modify
		20080201	PAGE19: change HDMI SCL/SDA pull res R168,R171,R163,R170 to 4.7K ,change R1,R2 to 6.8K	Circuit modify
		20080201	PAGE20: change Panel SDA/SDC pull res R412,R410 from 39K to 4.7K	Circuit modify
		20080204	ESD solution	Circuit modify
		20080204	PAGE23: add Varistor D63,D64,D65 on SPDIF_OUT/HP_JD/+3V_SPD	Circuit modify
		20080204	PAGE28: reserve D66 for CN36 , reserve D68,D69,D70 for FP , stuff D71,D72,D73 for BT	Circuit modify
		20080204	PAGE20:reserve D74,D75,D76 for CCD ,stuff D87 for LID switch	Circuit modify
		20080204	PAGE27:del R270,R597 , connect to +5V directly ,reserve D77~D81 for CN34(1ND HDD) ,reserve D82~D86 for CN32(2ND HDD) ,reserve D67 for CN31	Circuit modify
		20080204	PAGE26:reserve D88~D91 for 1394	Circuit modify
		20080204	PAGE04:reserve D92,D93 for FAN , reserve C795,C796 change R122 to 0 0603	Circuit modify
		20080204	PAGE13,19,21,25:reserve C797~800 for PLTRST#	Circuit modify
		20080204	PAGE04: pull up R691 CPU_BDREQ# to avoid noise cause system shut down	Circuit modify
		20080205	PAGE23:Change R714,R715 from 10uF to 0 ohm (Audio HP circuit)	Circuit modify
		20080210	PAGE18,29: DEL D4,D5 footprint and DEL CRT_SENSE# net, No stuff R218	Circuit modify
		20080210	PAGE28: DEL C42, Add D94 for CN8/Pin2 (ESD issue) - default no stuff	Circuit modify
		20080210	PAGE28: Change L70,L71 from CX216900002 to CX163210007	Circuit modify
20080210	PAGE28: Stuff L64,L65 to CX163210007	Circuit modify		
20080213	PAGE27: Add ESATA re-driver IC	Circuit modify		
20080213	PAGE25: Change the footprint of R33 and R330 from 1206 to 0805	Circuit modify		
20080213	EMI solution	Circuit modify		
20080213	PAGE18: C4,C7,C10,C5,C8,C11 change from 10p to 6.8p	Circuit modify		
20080213	PAGE28: stuff C391,C701, C559 ,C228,C465,C618,C41,C43, C618,C794,C809,C810	Circuit modify		
20080213	PAGE20: stuff C427~C432	Circuit modify		
20080213	PAGE30: stuff C39,C346	Circuit modify		
20080213	PAGE29: stuff C577,C578,C560	Circuit modify		
20080213	PAGE12: stuff C804~C807 for +NB_CORE	Circuit modify		
20080213	PAGE25: stuff C40,C36,C54,C58,C289,C352,C319,C272 for WL	Circuit modify		
20080213	PAGE19: stuff C808 for HDMI	Circuit modify		
20080213	PAGE15: stuff C375,C366 for SB HW MONITOR	Circuit modify		
20080213	PAGE22: stuff R627	Circuit modify		
20080213	PAGE26: change R683 from 0 to 33 ohm	Circuit modify		
20080214	UPDATE POWER	Circuit modify		
20080215	PAGE28: CN42 co-layout with CN16	Circuit modify		
20080215	PAGE31: Remove R98,R145,R118 Hole15,17,18	Circuit modify		
20080215	PAGE28: Change L70,L71 from CX216900002 to CX201290009	Circuit modify		
20080218	PAGE31: HOLE 15,24,25 FBBD3017010 change to FBBD3021010	Circuit modify		
20080218	PAGE31: HOLE 28,35 FBBL5007010 change to FBBL5050101 , HOLE 13,14 FBBL5008010 change to FBBL5051010	Circuit modify		



PROJECT : BD3G
Quanta Computer Inc.

Model	REV	DATE	CHANGE LIST	NOTE
BD3G	C3A	20080218	PAGE04: G781 reverse R718 0 ohm for Griffin CPU	Circuit modify
		20080219	PAGE04: change G781 to G786P81U	Circuit modify
		20080220	PAGE27:1.change C801,C82 from 0.01u to 4.7n, 2.RX add C811,C812 4.7n	Circuit modify
		20080222	PAGE15:change SATA ODD from port3 to port4 (solve ODD post detect fail)	Circuit modify
		20080226	PAGE27:change ESATA conn usb-2006109-11p,update p/n to DFHS11FR021	Circuit modify
		20080227	update power include EMI	Circuit modify
		20080229	del co-layout parts RN34,RN35,R608,R607,R572,R569	Circuit modify
		20080303	PAGE14: del Mini card USB10,Felica USB5 , change BT to port5 , ESATA to port 10	Circuit modify
		20080303	PAGE25: MINI PCI II no need USB , change USB10 to ESATA .and del R169,R188	Circuit modify
		20080303	PAGE28: no Felica request , remove USB del R178,R179,remove Q57,C476,R450,Q56	Circuit modify
		20080303	PAGE31: EMI request add C813,C814	Circuit modify
		20080410	PAGE17: change R150 to R152 for power sequence	Circuit modify
		20080410	PAGE26: add D88--D91 for 1394 ESD	Circuit modify
		20080410	PAGE27: change ESATA conn usb-2006109-11p update p/n to DFHS11FR023	Circuit modify
		20080410	PAGE27: add D67,D49,D50 for ESATA USB ESD	Circuit modify
		20080410	PAGE28: add D51,D52, D66 for USB0	Circuit modify
		20080410	PAGE34: add PC191,PC193 for CPU core	Circuit modify
		20080410	PAGE35: del PR81	Circuit modify
		20080410	PAGE27: remove Flash card ckt	Circuit modify
		20080416	PAGE13: change RTC pad location to G1	Circuit modify
		20080416	PAGE14: pull up USB_OC5# R719	Circuit modify
		20080416	PAGE18: update footprint to sv-030018fr004s100fr-4p-h-bl5m	Circuit modify
		20080416	PAGE23: update footprint to knob-xre094-3p-bl5m	Circuit modify
		20080416	PAGE28: remove CN42 not co-layout with CN16	Circuit modify
		20080416	PAGE31: update HOLE13,14 footprint to H-C236D146P2	Circuit modify
		20080417	PAGE27: remove D77--D81 for CN34 , change to U44 CM1213-04SO(AL001213001) ,remove D82--D86 for CN32 , change to U45 CM1213-04SO	Circuit modify
		20080418	PAGE28: Change L72 from CX163210007(BT circuit) to CX201290009	Circuit modify
		20080421	PAGE31: remove Hole31,37	Circuit modify
		20080421	no stuff +3VSUS component	Circuit modify
			PAGE31: no stuff C229,C518,C128	Circuit modify
			PAGE33: no stuff PQ23	Circuit modify
			PAGE37: no stuff PR95,PQ20	Circuit modify
		20080424	PAGE16: IDE/FLASH not use ,remove C287,C288,C297,C293,C294	Circuit modify
		20080424	PAGE16: internal clk not use ,remove C332,C330,C327,C331, change L28 to 0 ohm	Circuit modify
		20080424	To meet ESATA SI PAGE27: change R706 from 0 ohm to 330 , stuff R692,R693,R694	Circuit modify
		20080424	PAGE16: remove C762 to meet PWRGD timing spec	Circuit modify
		20080424	PAGE9: stuff R480,R479 to meet AMD spec	Circuit modify
		20080424	PAGE17: stuff C765 10nf to meet power sequence	Circuit modify
		20080505	PAGE34: intersil recommand to set OCP to 30A Change PR218 from CS32052FB21 to CS41072FB11,Change PR157 from CS41002FB28 to CS31002FB26,Change PR160 PR216 from CS31622FB27 to CS23652FB08	Circuit modify
		20080505	PAGE22: Change CN17 from DFHD04MR021 to DFHD04MRA75	Circuit modify
		20080505	PAGE27: update re-driver footprint to tqfn36-5x6-5-37p-0_75h-te1m	Circuit modify
		20080505	PAGE20: reserve R720,R721 for cost down	Circuit modify
		20080505	PAGE27: add C816 0.1u to U44 +5V for ESD , add C818 0.1u to U45 +5V for ESD	Circuit modify
		20080505	PAGE25: remove CN30 second PCIE (HD Decoder)	Circuit modify
		20080505	PAGE31: remove HOLE28,35 (HD Decoder)	Circuit modify
		20080507	PAGE20: stuff D74,D75,D76 for CCD	Circuit modify
		20080508	PAGE20: reserve CM1293 U46,C819 for CCD ESD protect	Circuit modify
		20080508	PAGE28: stuff D68,D69,D70 for FP	Circuit modify
		20080508	PAGE30: stuff D53 for RF_LED ESD	Circuit modify
		20080509	PAGE26: 5/9 for card reader MS DUO adapter short issue reserve R723,724,722 ,Q82,Q81,Q83,Q84	Circuit modify
20080513	PAGE4: follow AMD design guide 1.03 stuff R675	Circuit modify		
20080527	PAGE26: some 1394 device can't boot normal change L38 to BK1608HS220_6	Circuit modify		
20080527	PAGE34: CPU core adj 1.PR160,PR216 change to 3.92K/F_4 2.PR213,PR215 change to 18.2K/F_4	Circuit modify		
20080527	PAGE33: solve system hang up , when plug adp quickly change PR113 from 150K_4 to 115K/F_4	Circuit modify		
20080527	PAGE33: avoid right side USB voltage drop change PR119 to 63.4K , PR120 to 10K	Circuit modify		
20080528	PAGE12: del C805,C807	Circuit modify		
20080529	PAGE27: change ESATA conn p/n to DFHS11FR027	Circuit modify		